

# AMD TR4(X399)

## Promontry X370

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# MS-7B92 Ver:10

**CPU:**  
AMD TR4

**System Chipset:**  
Promontory X399  
(XPOWER Enthusiast GAMING/SLI PLUS)

**Main Memory:**  
DDR IV \* 8 MAX:256 GB

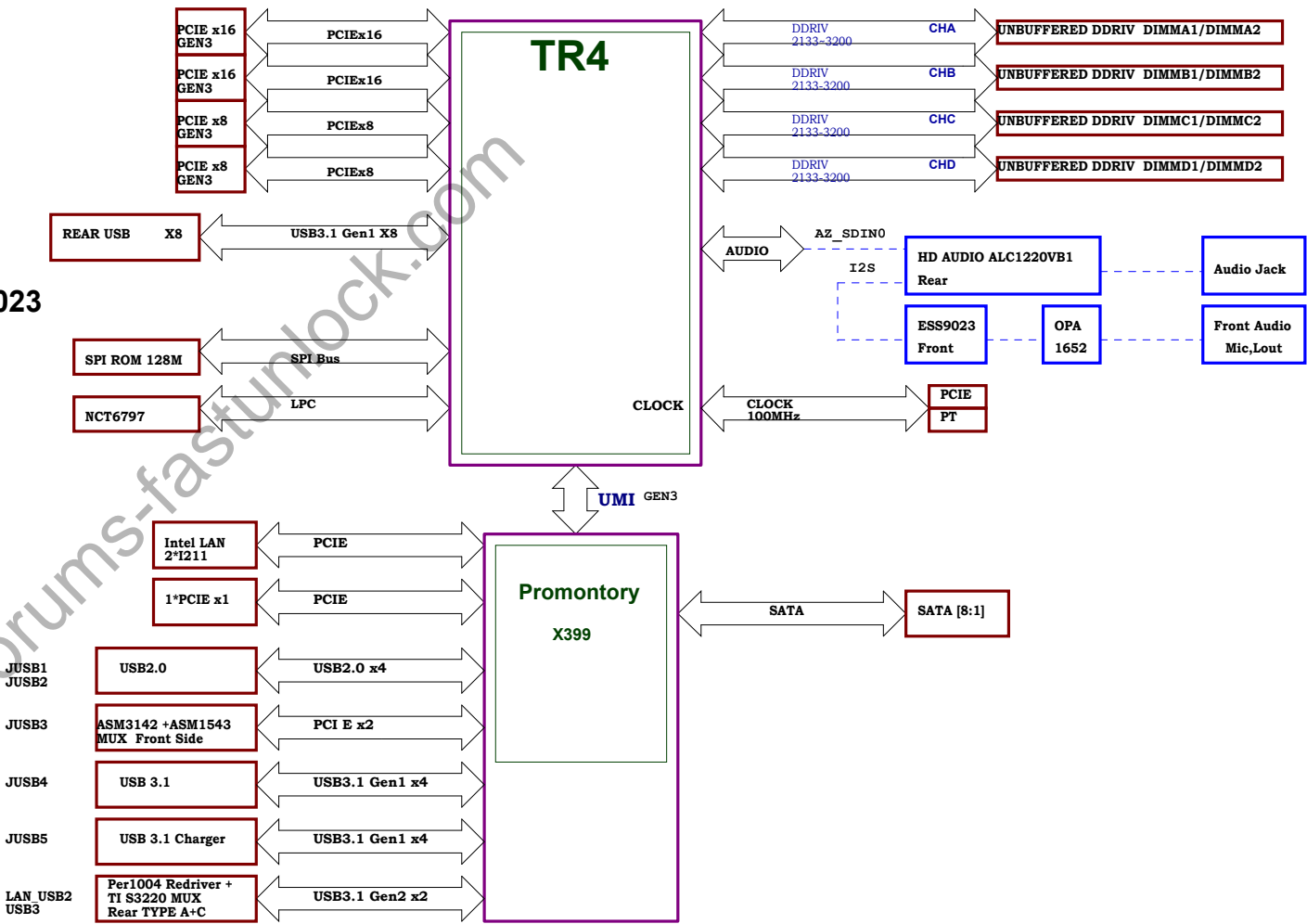
**VRM**  
IR35201-16Phase  
IR35204-3Phase

**On Board Chipset:**  
LPC Super I/O --NCT6797  
LAN Intel 211AT\*2  
Azalia CODEC - Realtek ALC1220P-VB + ESS 9023  
ASM3142 +ASM1543 MUX Front Side

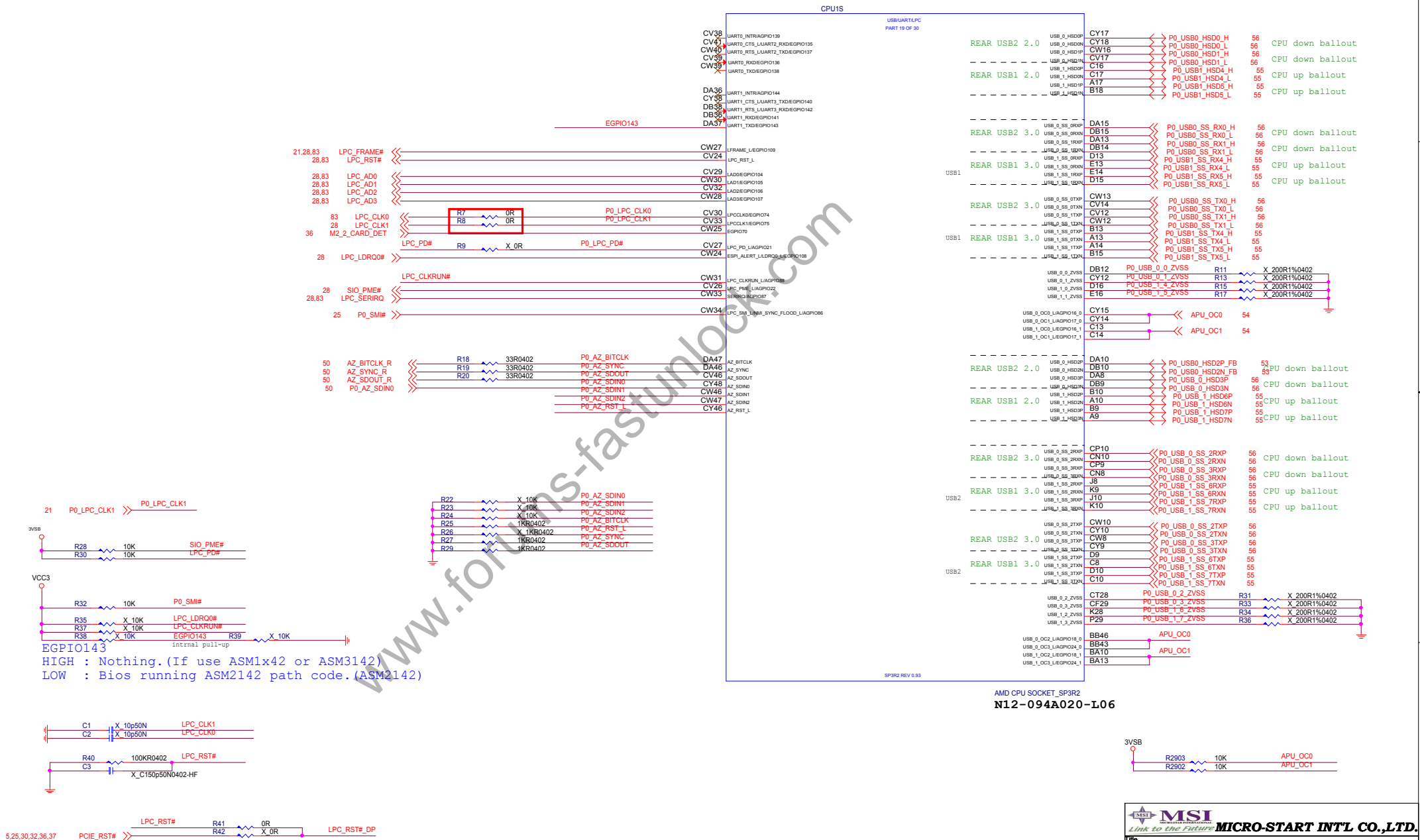
**Expansion Slots:**  
From CPU  
PCI Express X16 Slot \* 2  
PCI Express X8 Slot \* 2

From FCH  
PCI Express X1 Slot \* 1

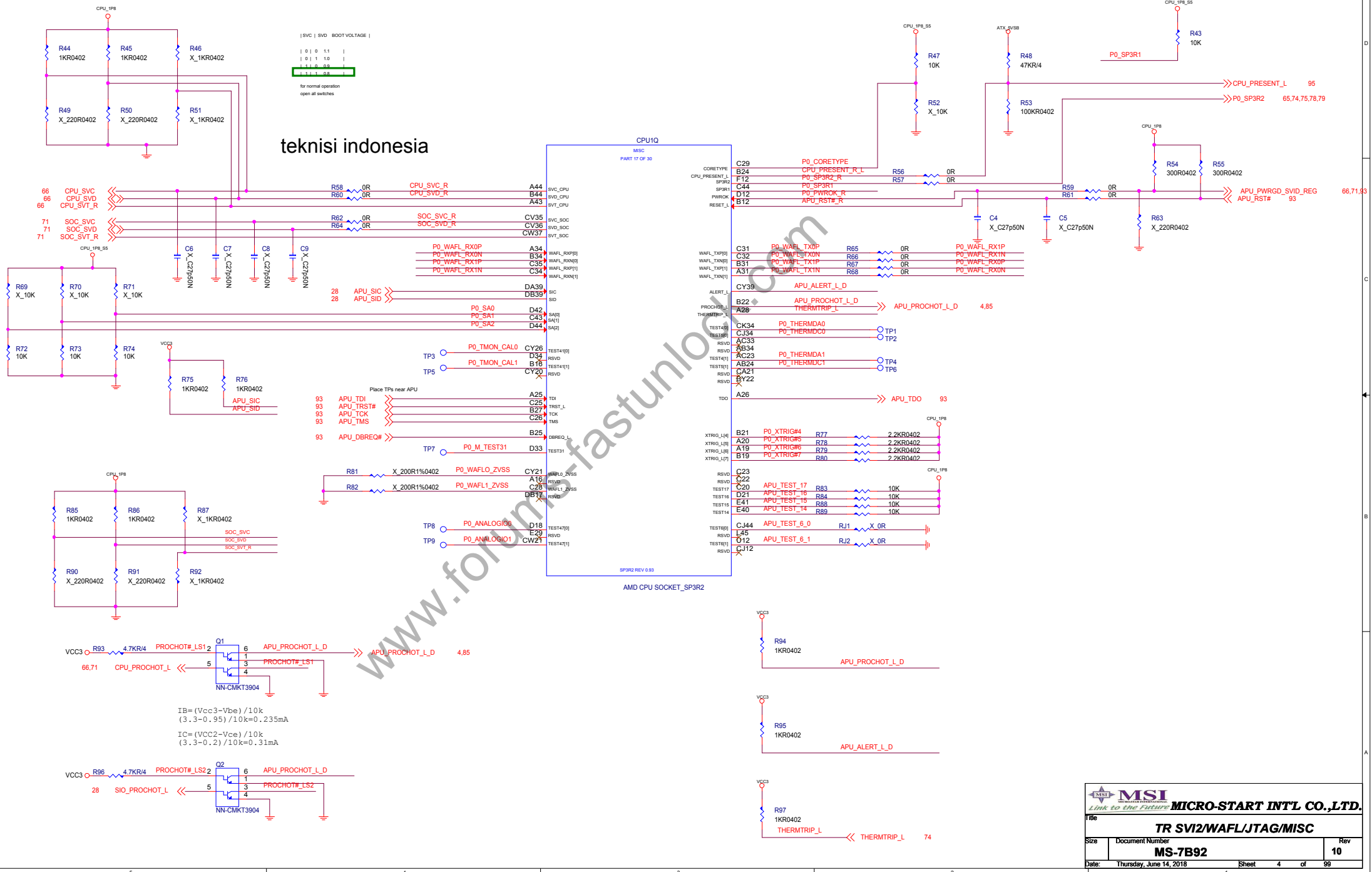
## X499 BLOCK DIAGRAM



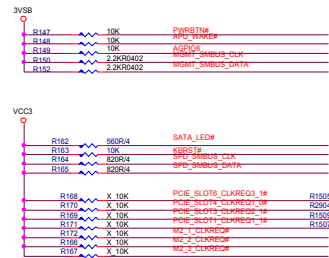
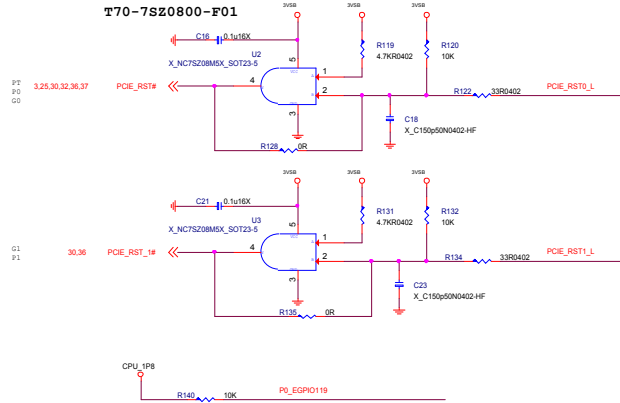
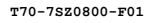
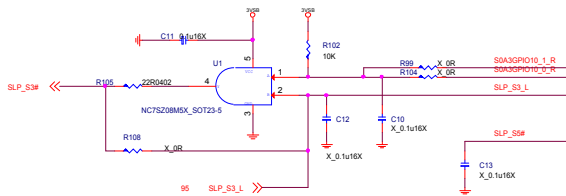
## USB/LPC/UART/HDA



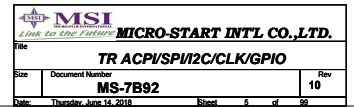
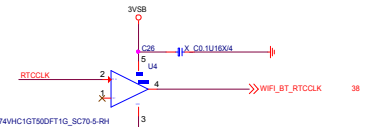
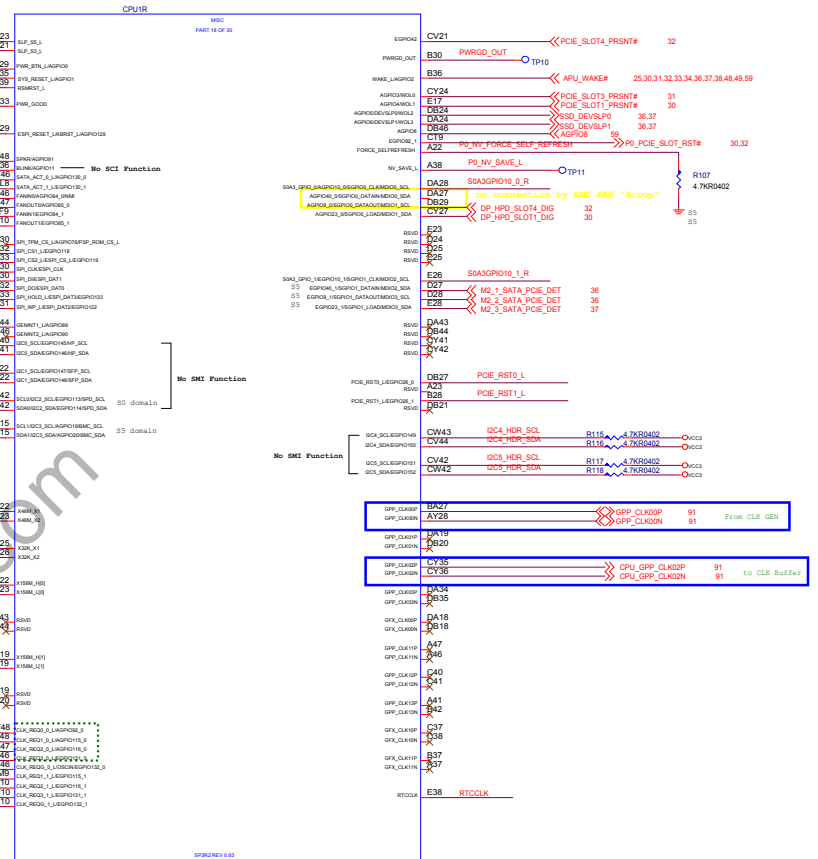
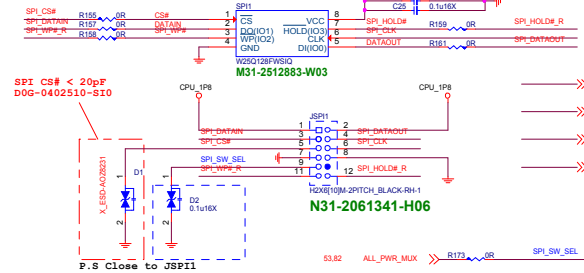
## SVI2/WAFL/JTAG/MISC



## ACPI/SPI/I2C/CLK/GPIO



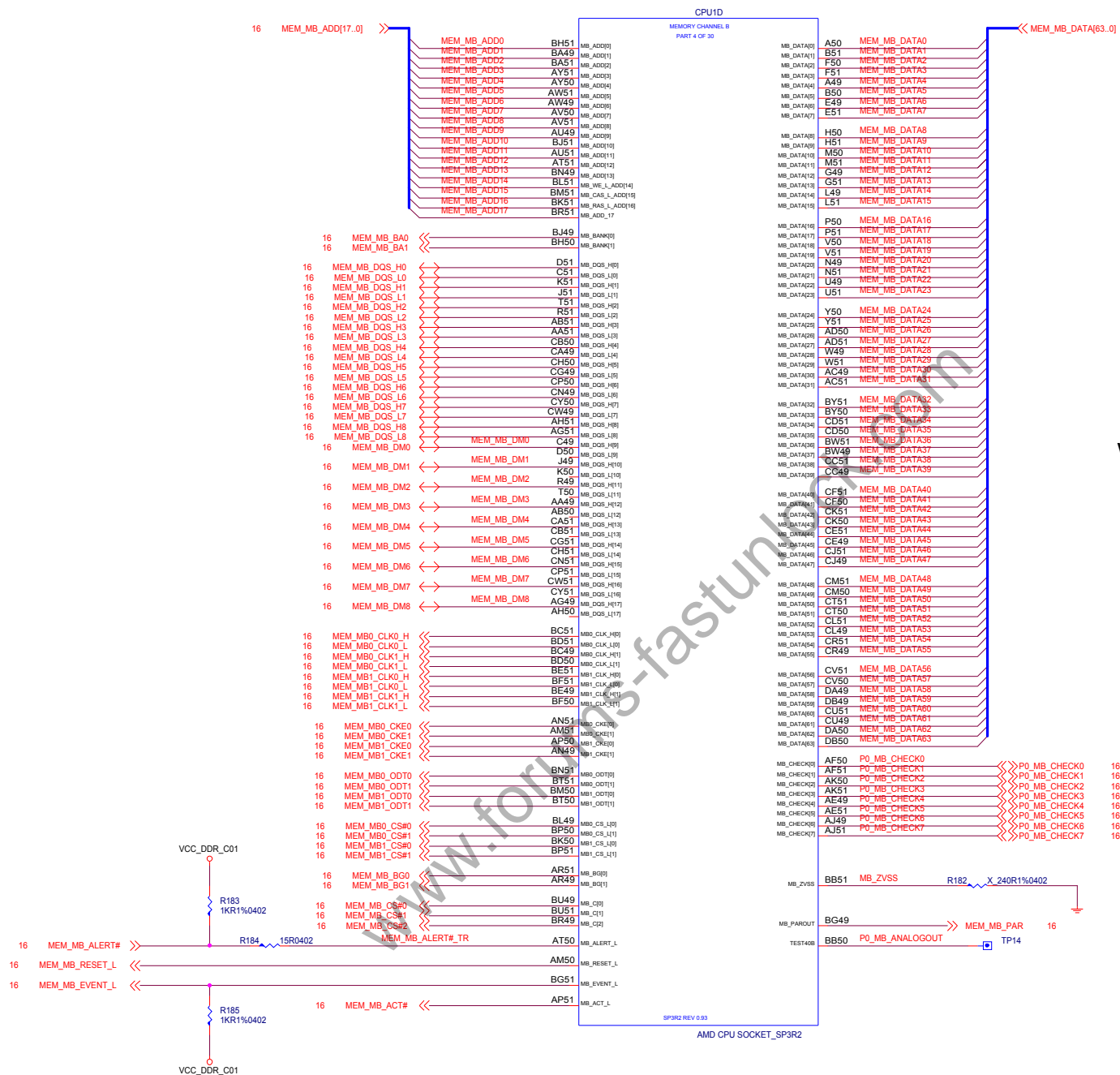
**SPI ROM (1.8V)**





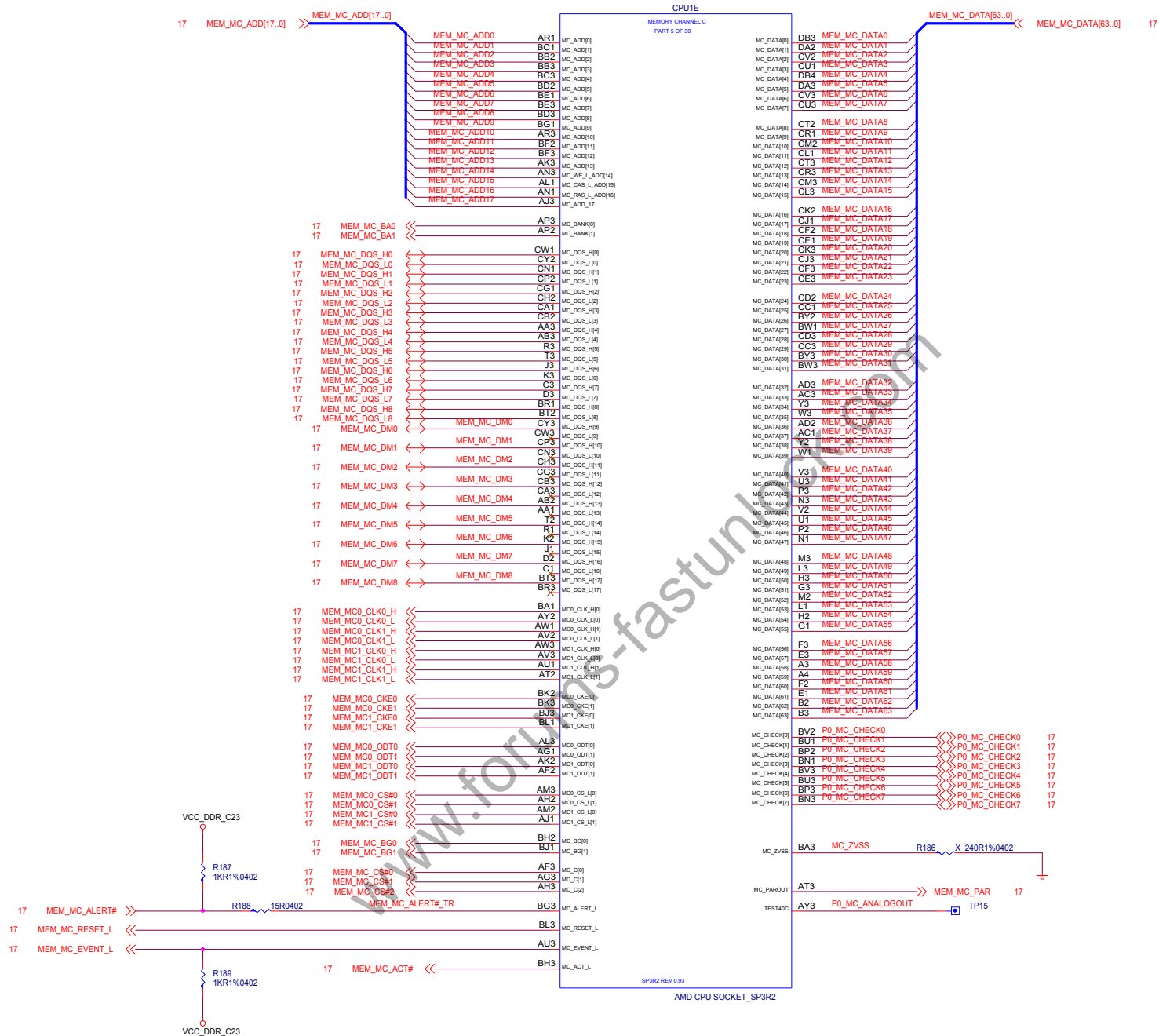






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# POWER



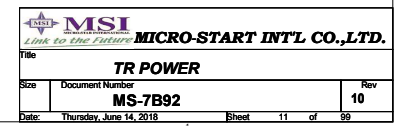
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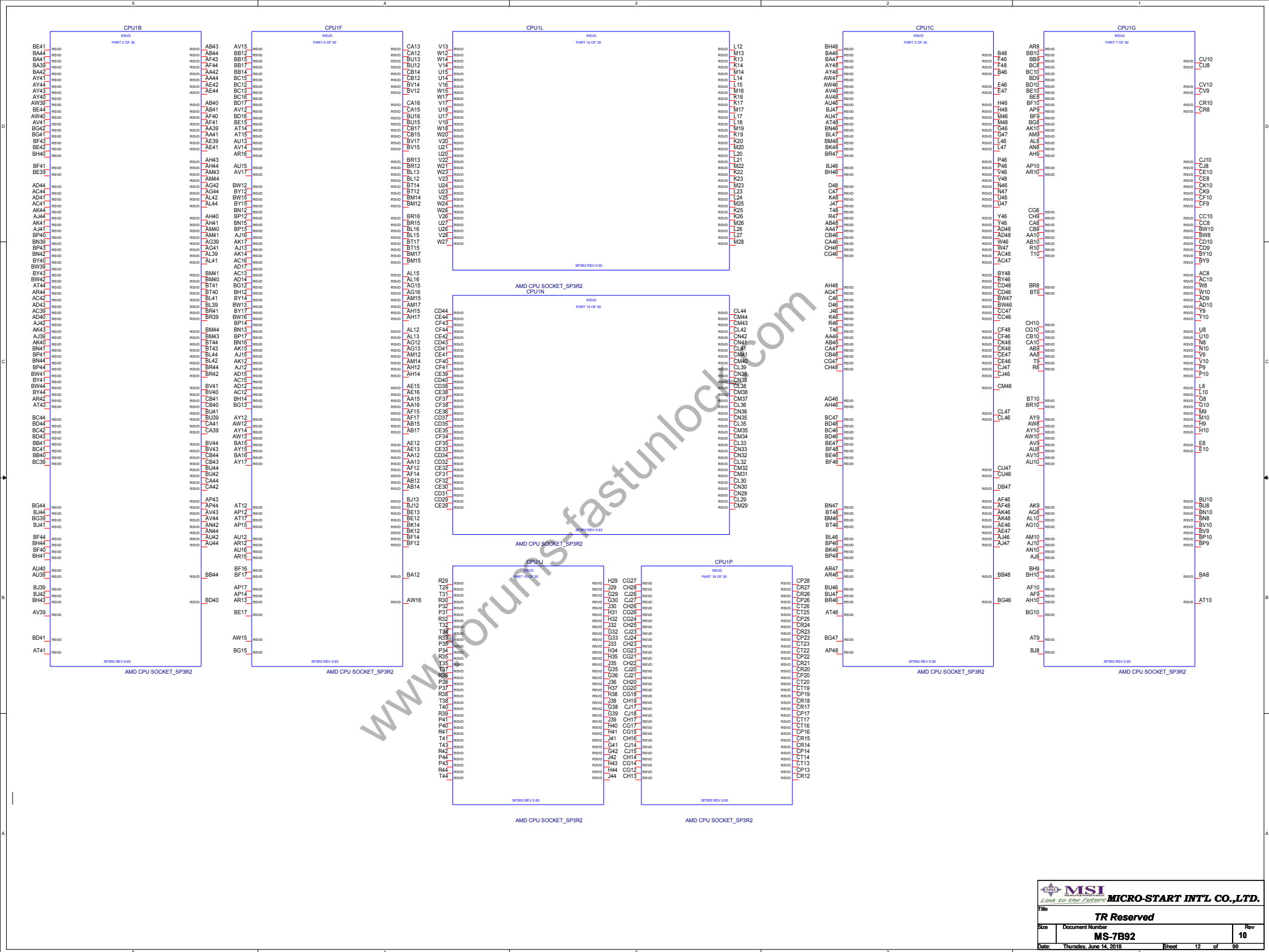
VDD0: 180A(TDC)245A(EDC);OC:260A(TDC)264A(EDC)
VDDSOC: 60A(TDC)85A(EDC)
VDDCR_SOC_SS: 2A(TDC/EDC)
VDDIO_MEM_AB: 15A(TDC/EDC)(CPU);45A(TDC/EDC)(MEMORY)-EXCEPTED THIS INCLUDES OC
VDDIO_MEM_CD: 15A(TDC/EDC)(CPU);45A(TDC/EDC)(MEMORY)-EXCEPTED THIS INCLUDES OC
VDD_1.5V: 3A(TDC)3A(EDC)
VDD_1.5V_SS: 1A(TDC)1A(EDC)

```

AMD CPU SOCKET\_SP3R2

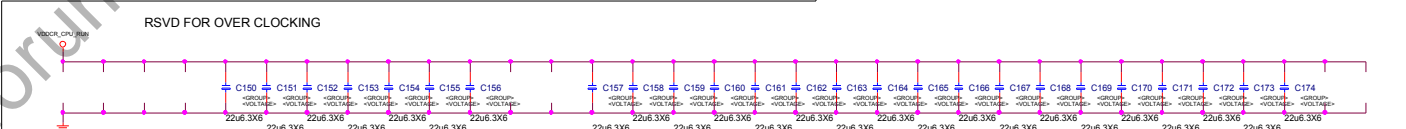
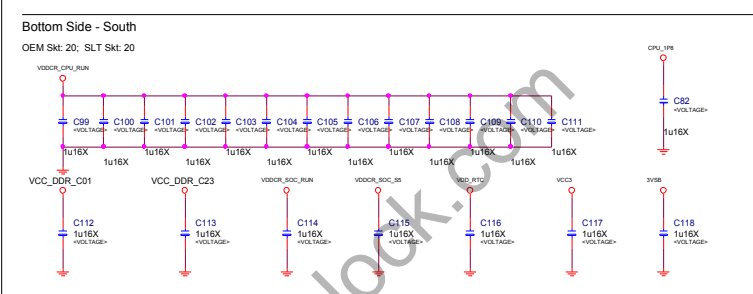
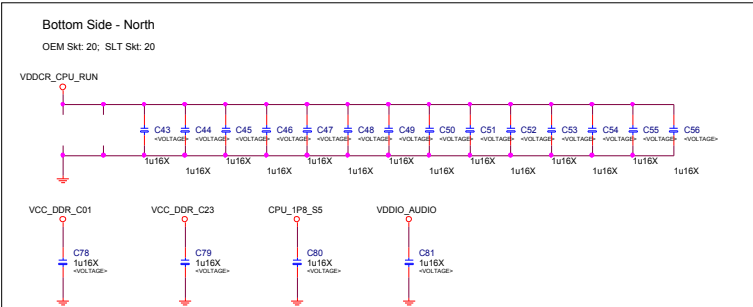
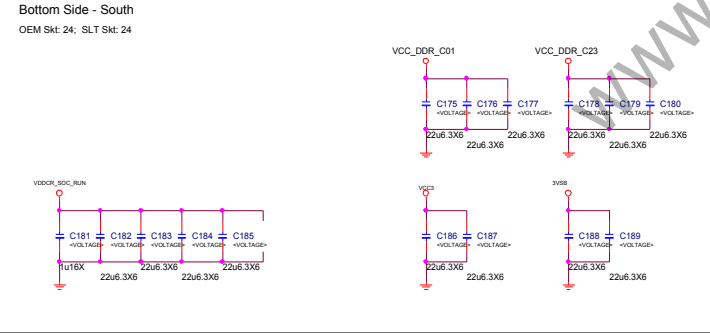
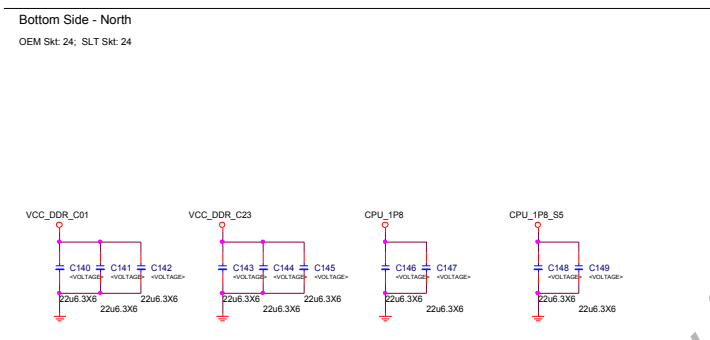
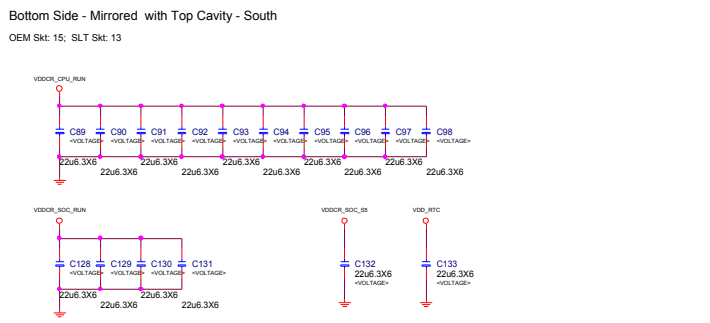
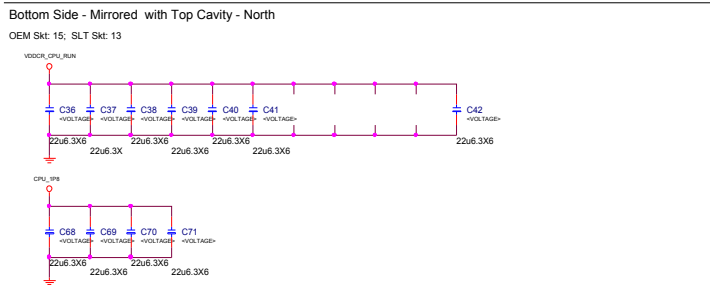
AMD CPU SOCKET SP3R:



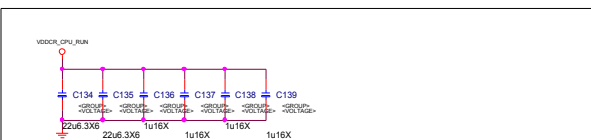
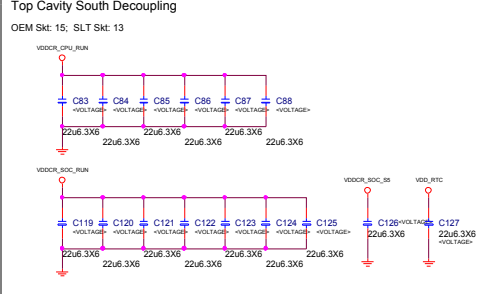
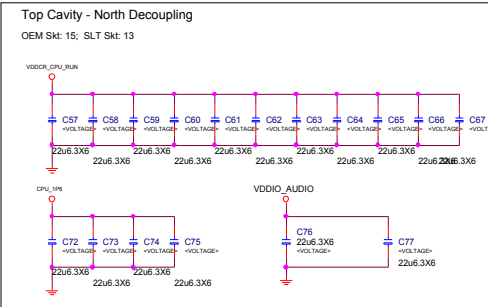


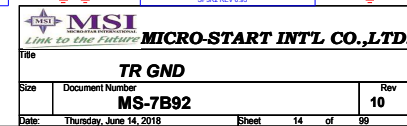
Decoupling Grouped by Placement Location

VDDCR\_CPU Bottom Side Decoupling:



Top Side Decoupling:







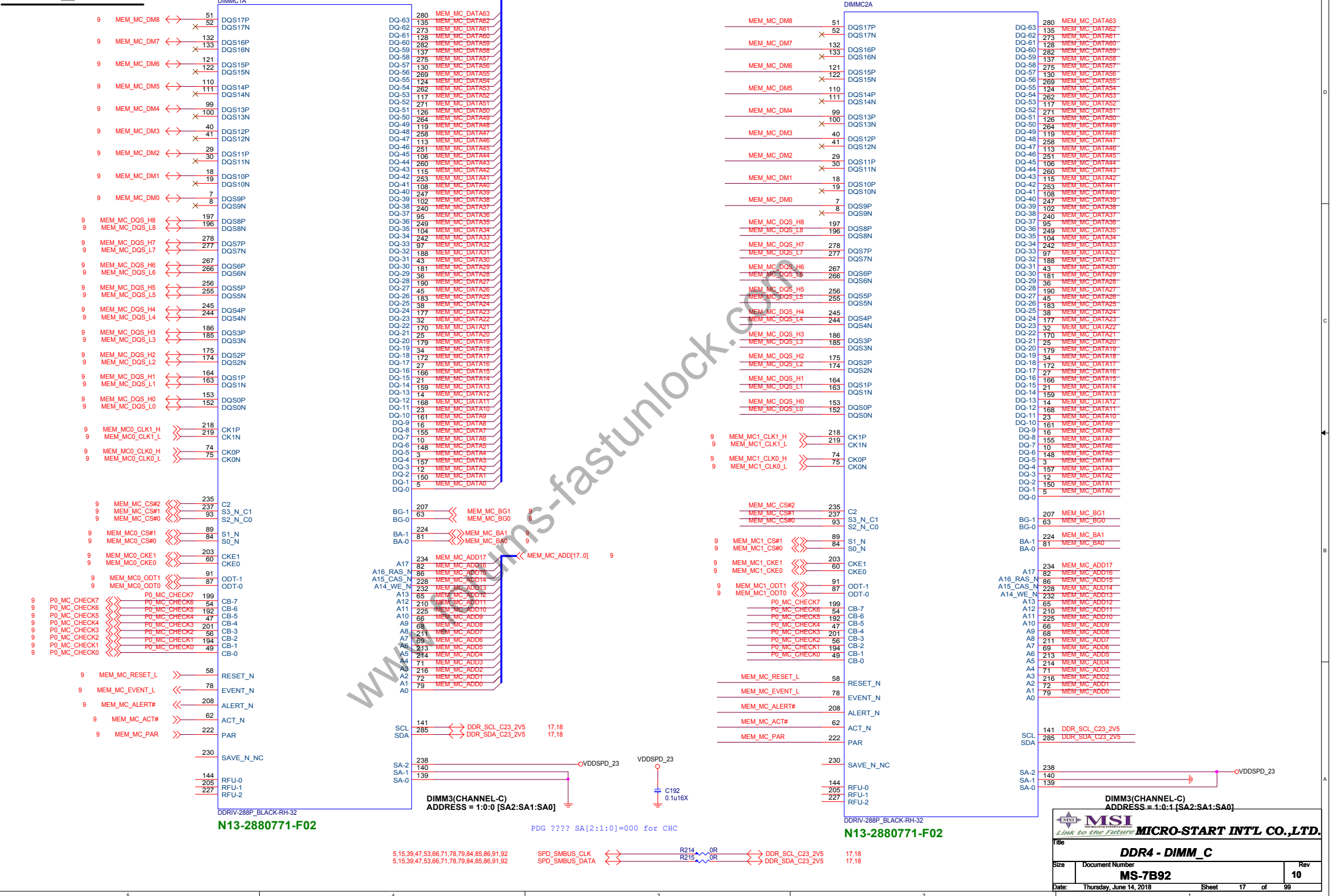




DIMM\_B1/B2



DIMM\_C1/C2



**MSI**  
Link to the future  
**MICRO-START INTL CO.,LTD.**

File: **DDR4 - DIMM\_C**

Size: Document Number: **MS-7B92** Rev: **10**

Date: Thursday, June 14, 2018 Sheet: 17 of 99

DIMM\_D1/D2



DDRIV-288P\_BLACK-RH-32

N13-2880771-F02

DIMM4(CHANNEL-D)  
ADDRESS = 1:1:0 [SA2:SA1:SA0]

PDG v0.7 P.158 SA[2:1:0]=010 for CHB

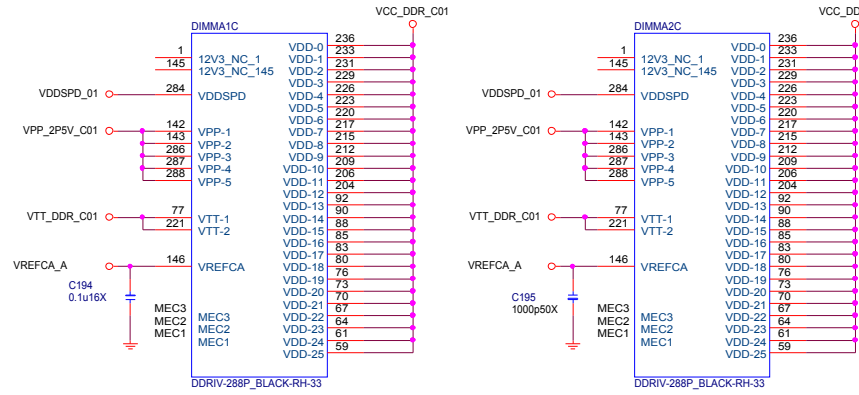
DDRIV-288P\_BLACK-RH-32

N13-2880771-F02

DIMM4(CHANNEL-D)  
ADDRESS = 1:1:1 [SA2:SA1:SA0]

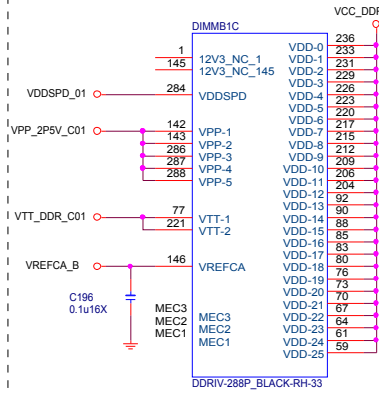
MSI MICRO-START INTL CO.,LTD.

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Size	Document Number	Rev			
			MS-7B92		
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**N13-2880811-F02**

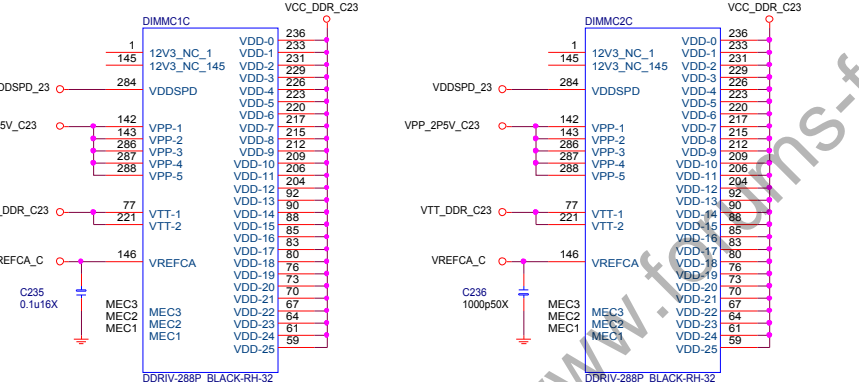
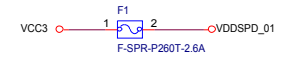
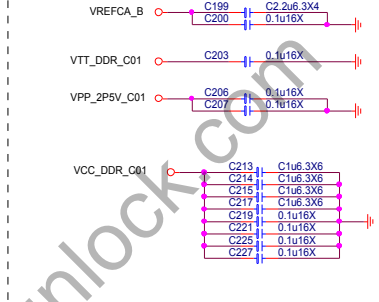
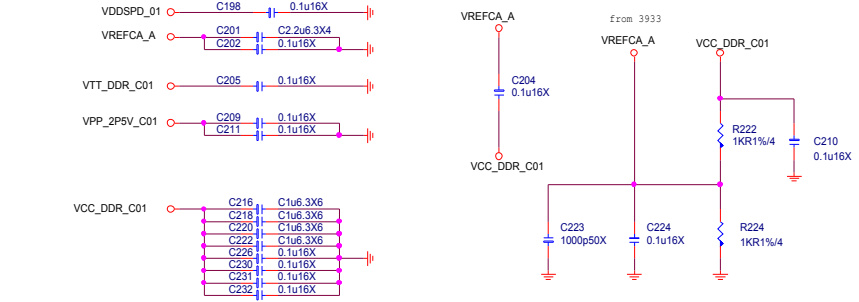
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**N13-2880811-F02**

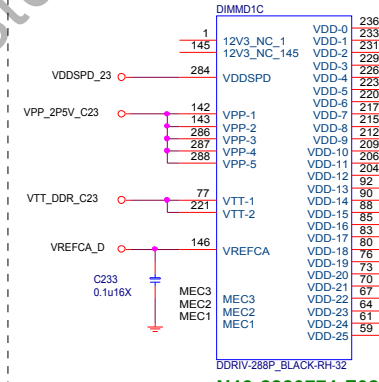
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**DDR VREF**  
(place resistors close to DIMMs)



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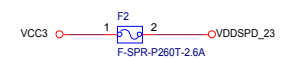
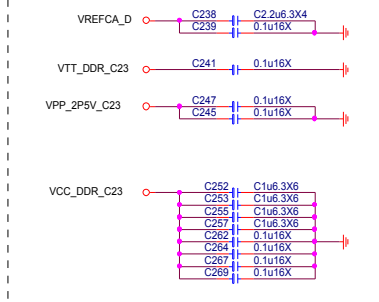
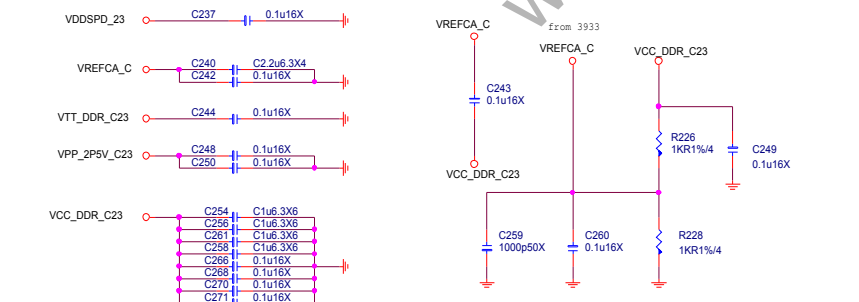
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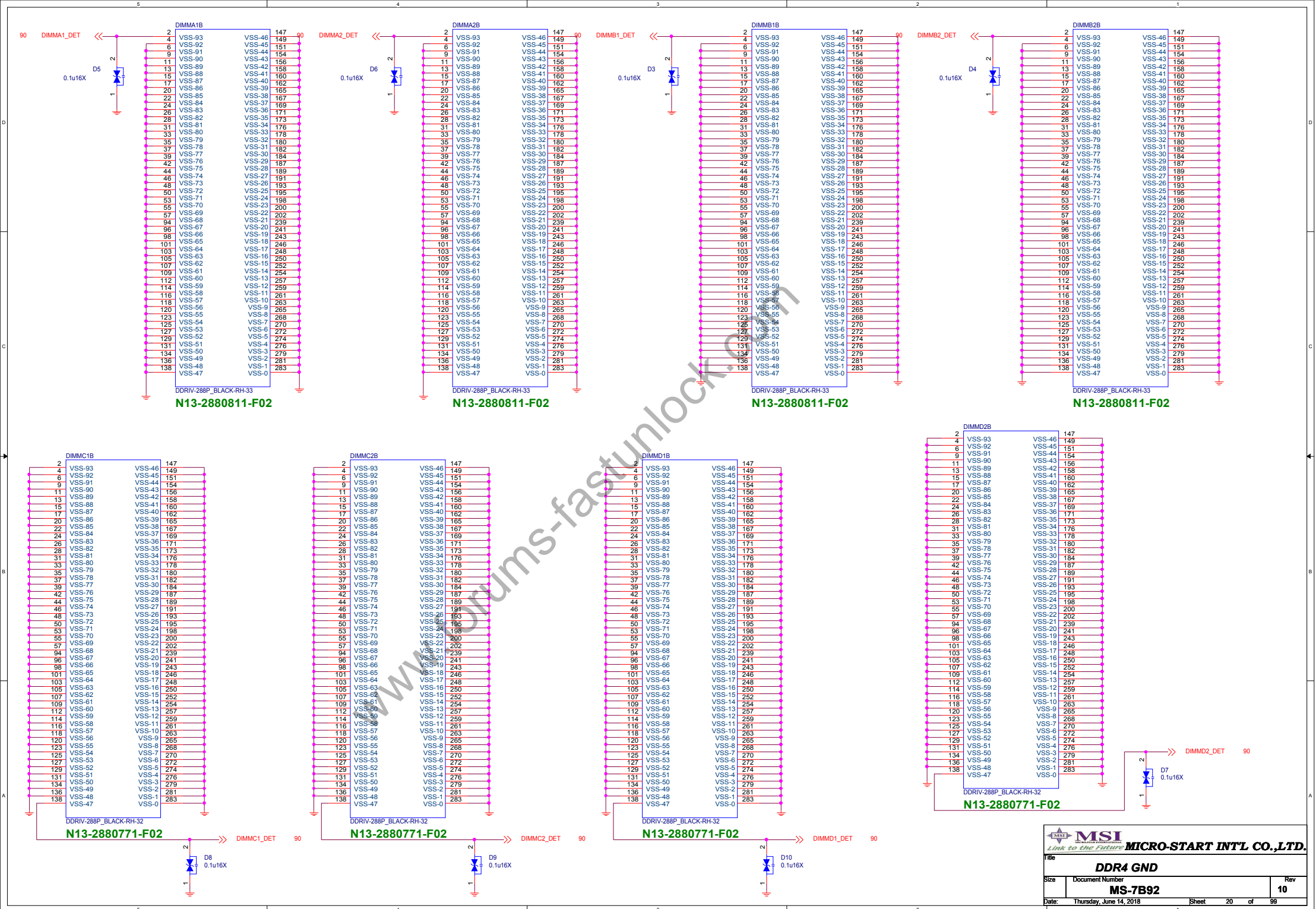
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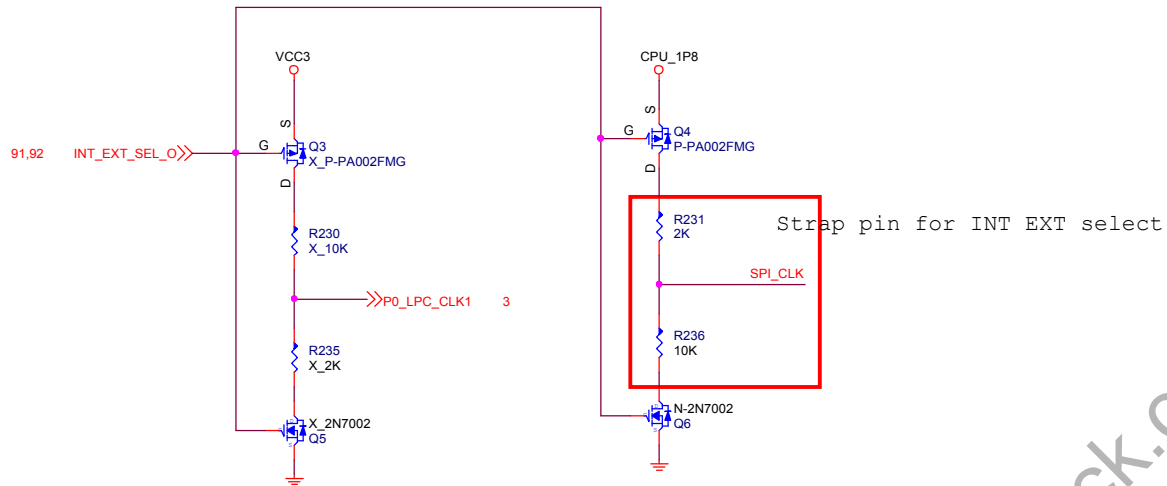
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**DDR VREF**  
(place resistors close to DIMMs)



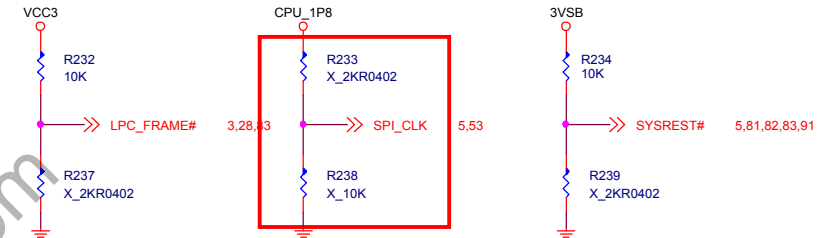
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Size	Document Number	Rev
	<b>MS-7B92</b>	<b>10</b>
Date:	Thursday, June 14, 2018	Sheet 19 of 99



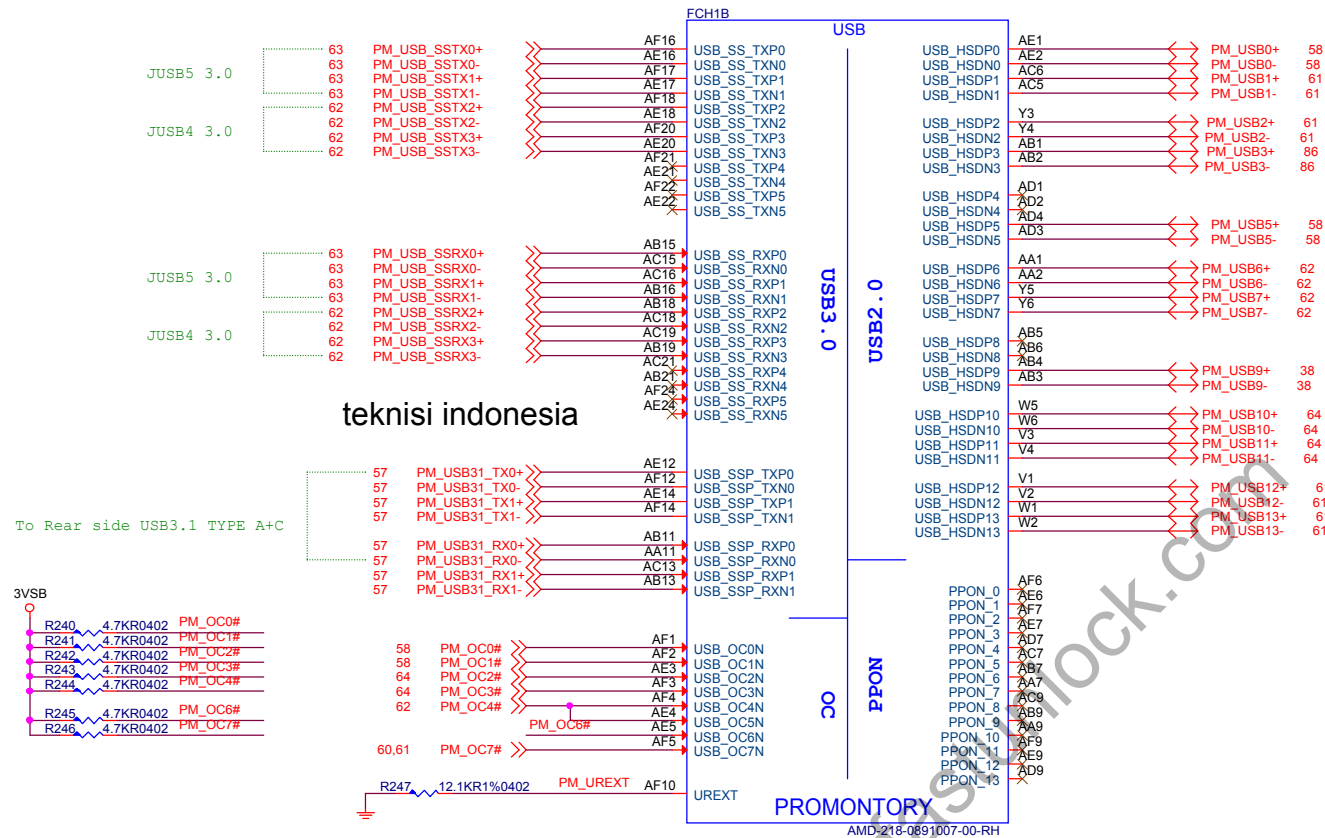


## CPU STRAPS

STRAP	DEFINITION
SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE
LPC_FRAME_L	ROM TYPE SELECT 1:BOOT FROM SPI ROM(DEFAULT) 0:BOOT FROM LPC ROM







## Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP[N]0	USB_HSDP[N]5	USB_OC0N
USB_SSP_TX/RXP[N]1	USB_HSDP[N]0	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SSP_TX/RXP[N]0	USB_HSDP[N]10	USB_OC2N
USB_SSP_TX/RXP[N]1	USB_HSDP[N]11	USB_OC3N
USB_SSP_TX/RXP[N]2	USB_HSDP[N]6	USB_OC4N
USB_SSP_TX/RXP[N]3	USB_HSDP[N]7	USB_OC5N
USB_SSP_TX/RXP[N]4	USB_HSDP[N]8	USB_OC6N
USB_SSP_TX/RXP[N]5	USB_HSDP[N]9	USB_OC7N
	USB_HSDP[N]1	USB_OC7N
	USB_HSDP[N]2	USB_OC7N
	USB_HSDP[N]3	USB_OC7N
	USB_HSDP[N]4	USB_OC7N
	USB_HSDP[N]12	USB_OC7N
	USB_HSDP[N]13	USB_OC7N

## Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

**MSI** MICRO-START INT'L CO., LTD.

Link to the future

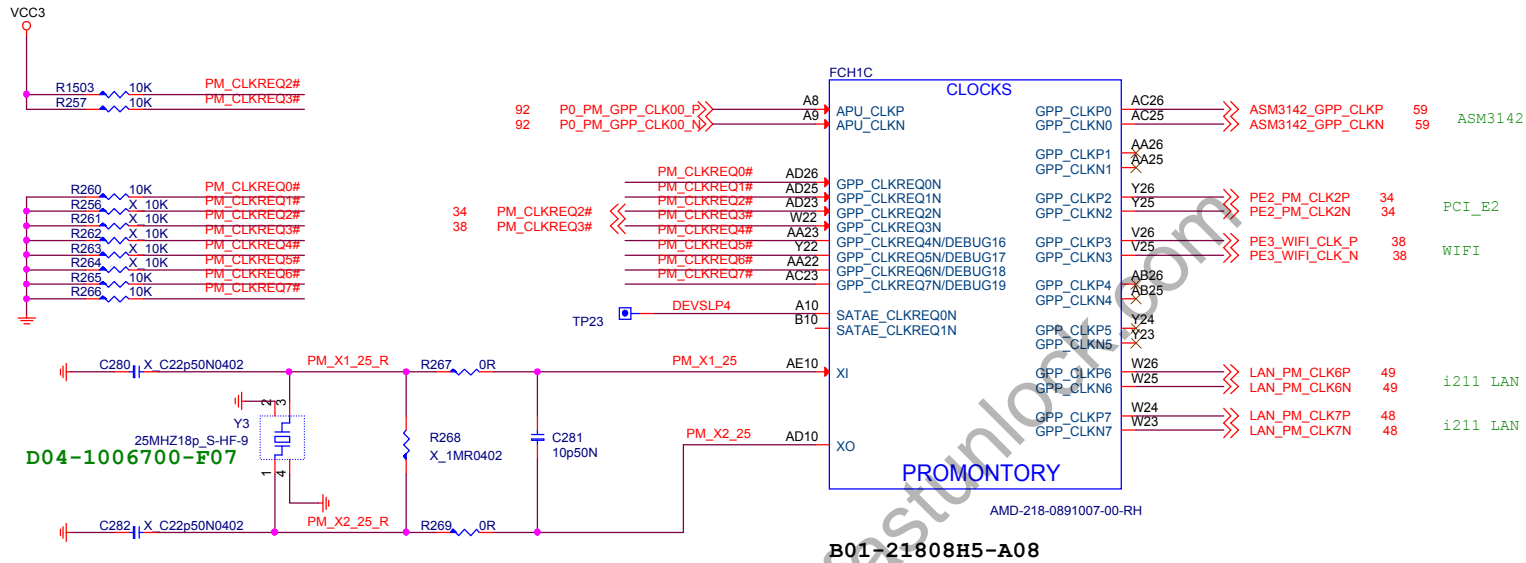
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Size: Document Number **MS-7B92** Rev **10**

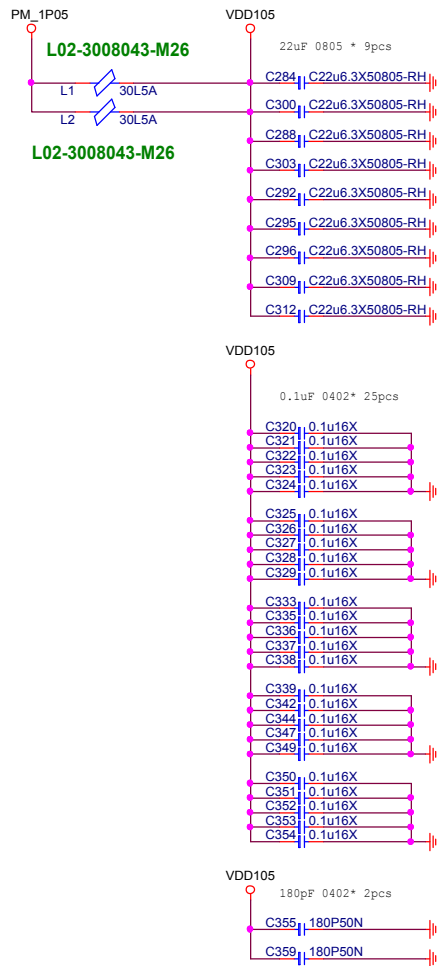
Date: Thursday, June 14, 2018 Sheet 22 of 99







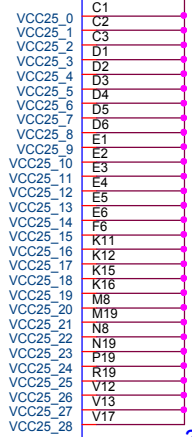




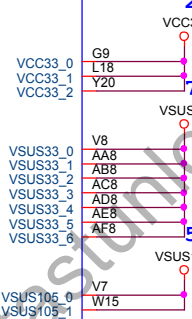
5.5A



POWER



900mA



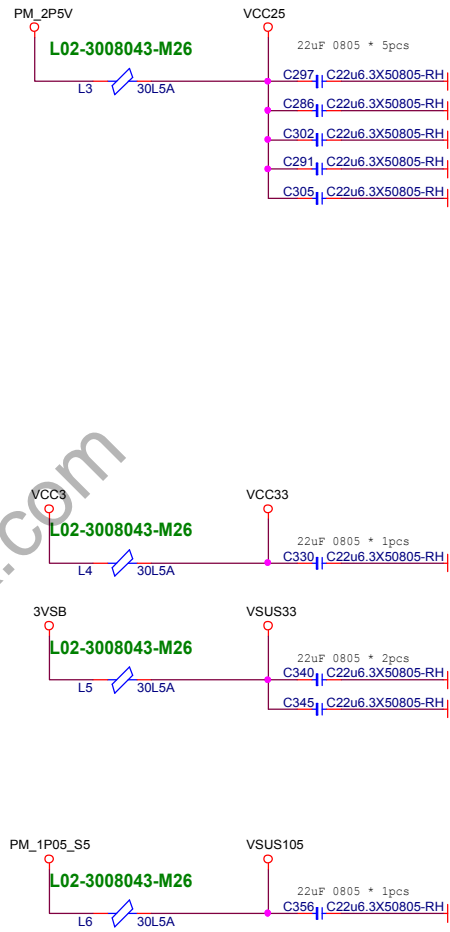
200mA

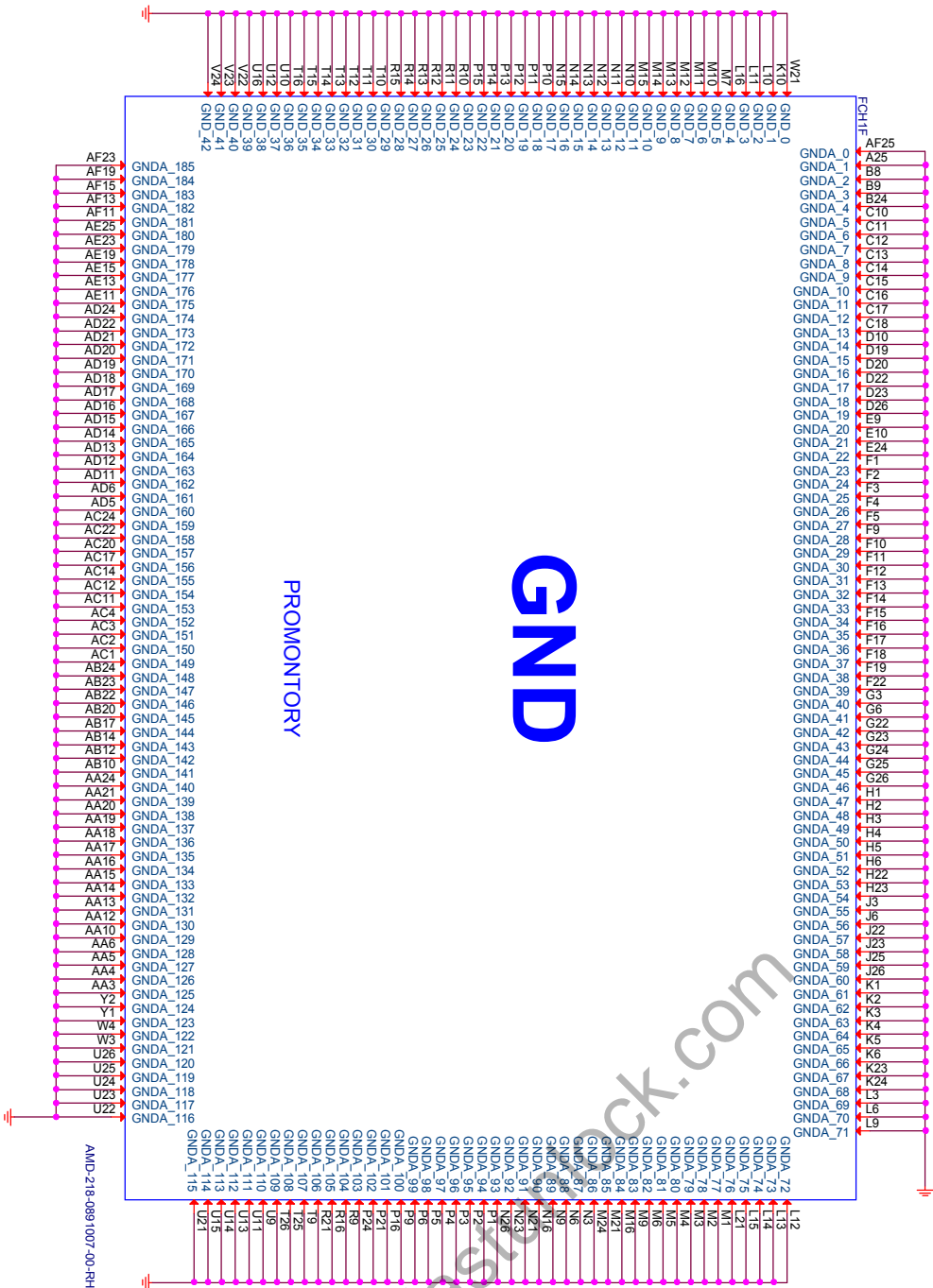
70mA

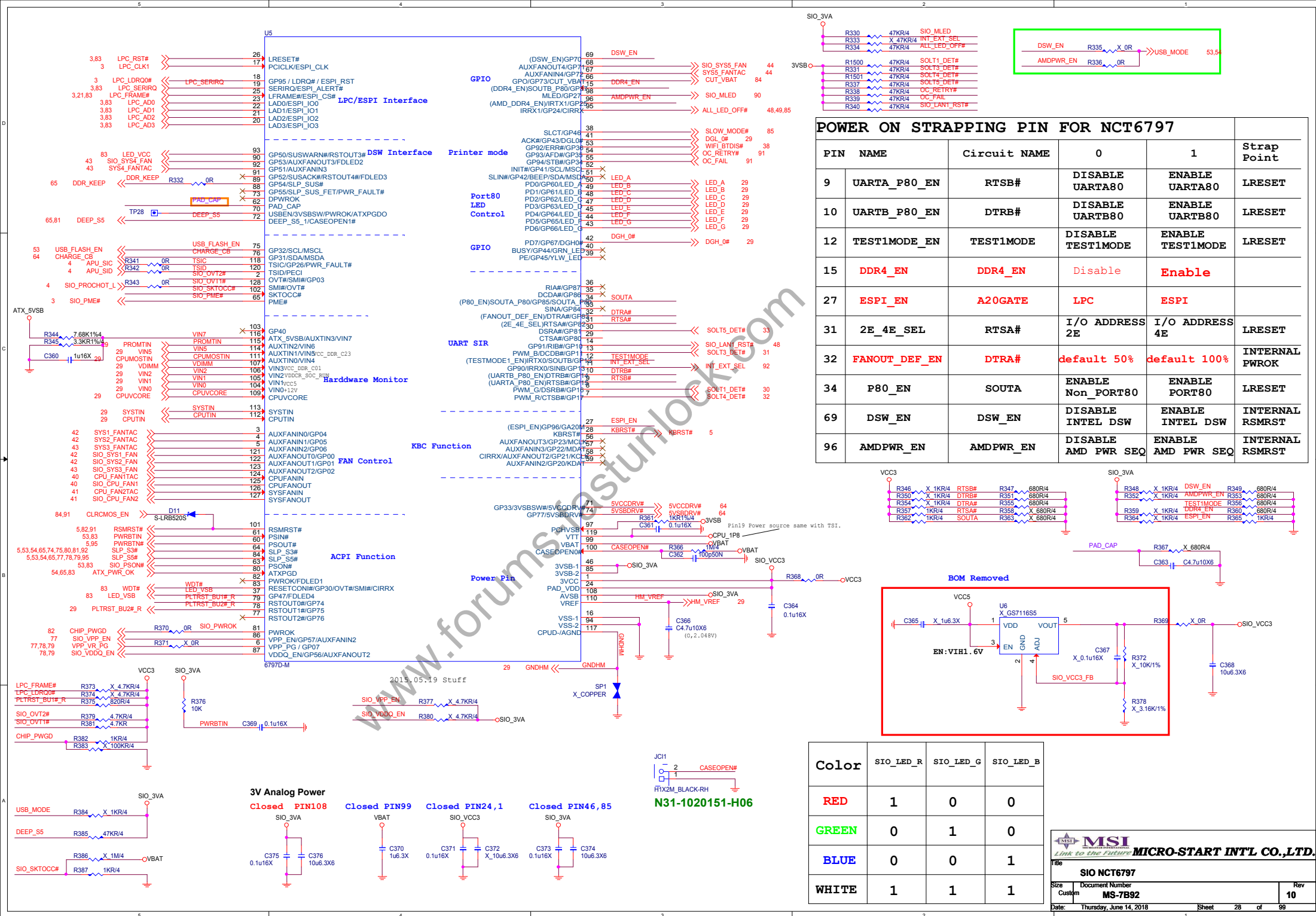
50mA

PROMONTORY

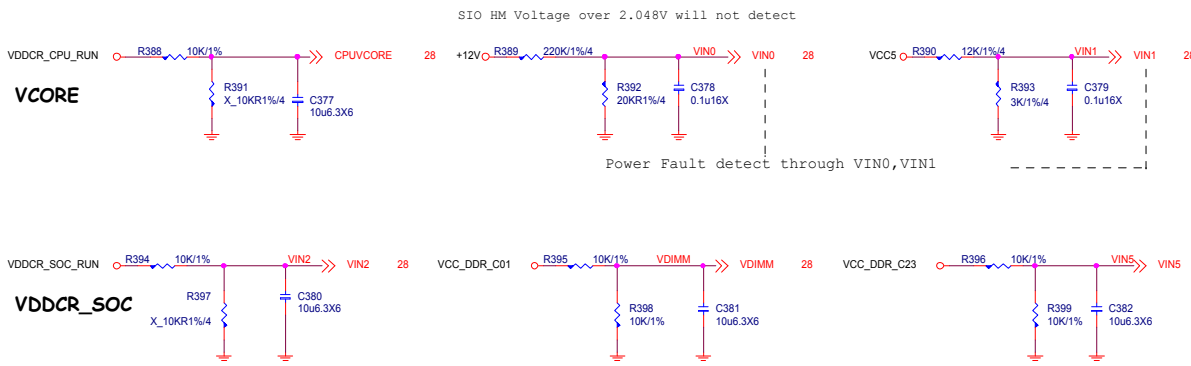
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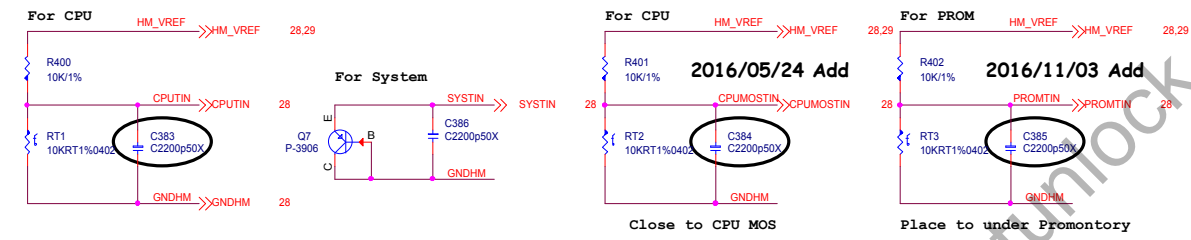




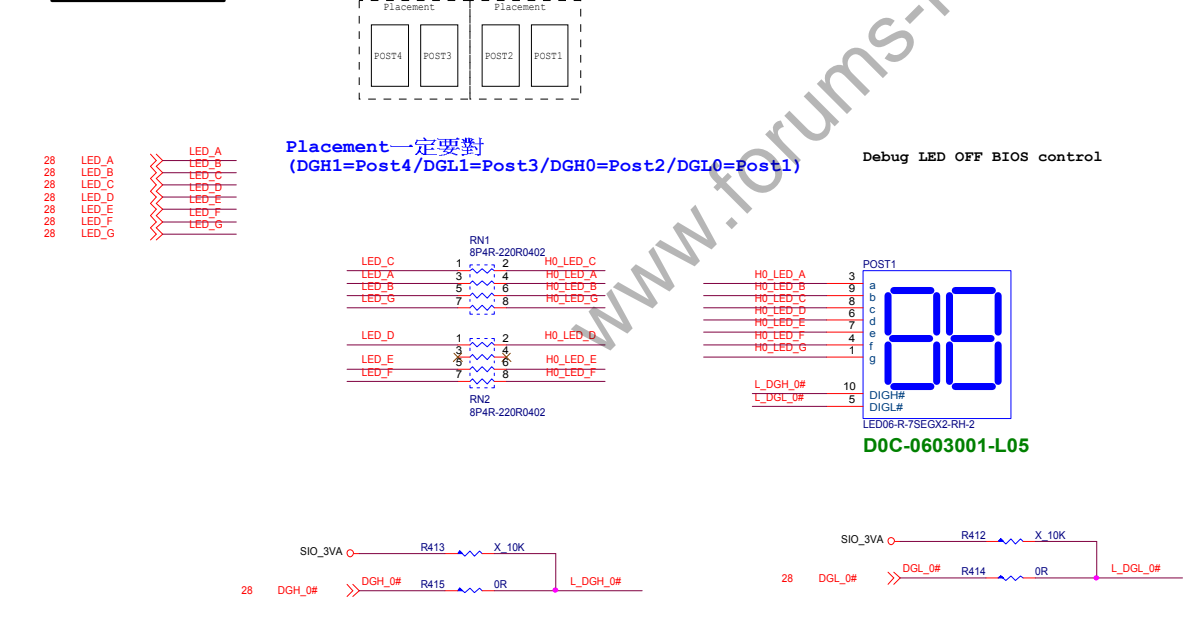
HW Monitor - Voltage



TEMP SENSOR



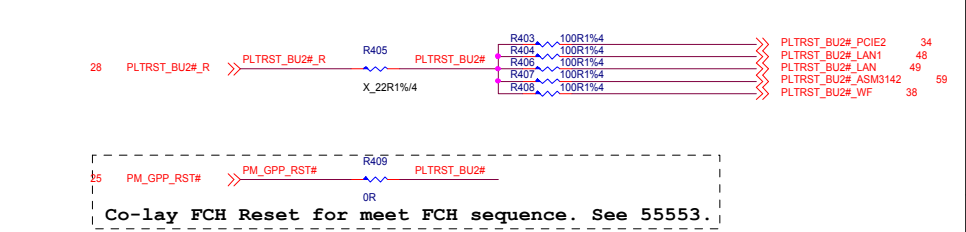
DEBUG LED



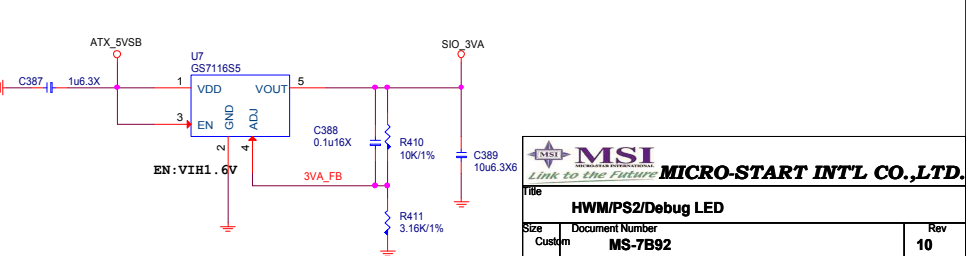
COM PORT

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RESET



SIO\_3VA

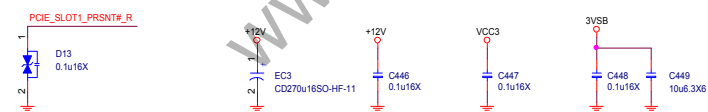




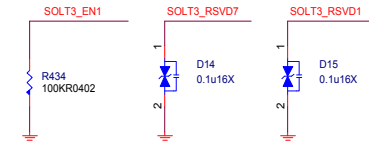
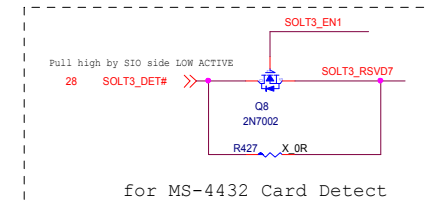
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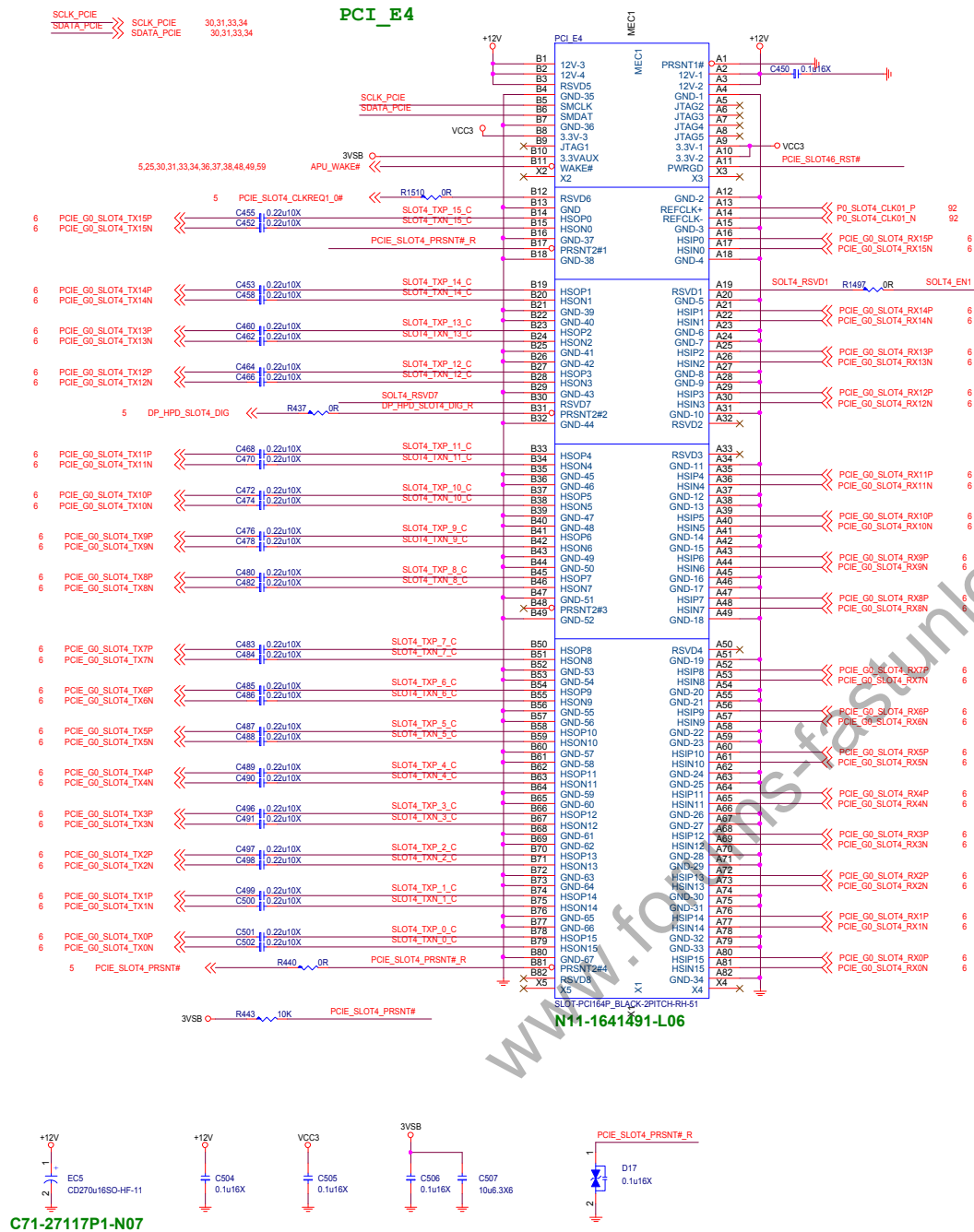
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**PCI EXPRESS X8 SLOT**

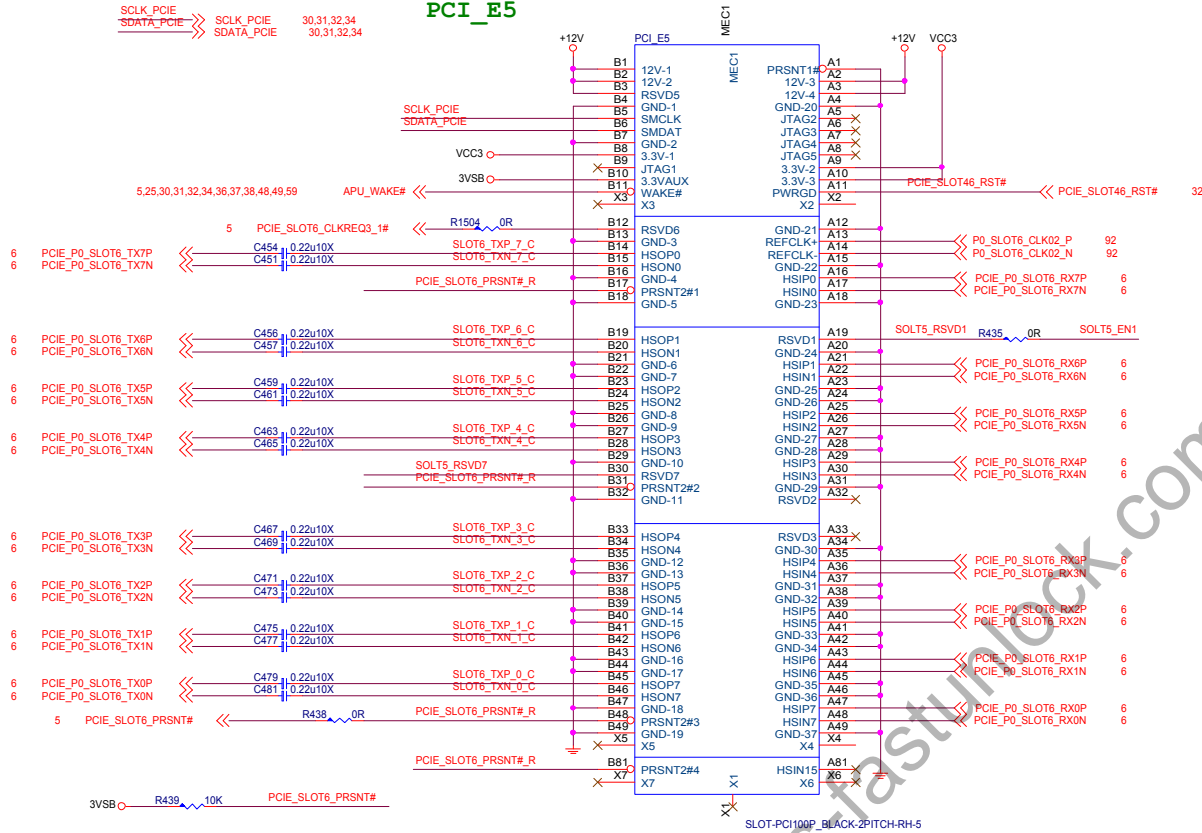


# PCI EXPRESS X16 SLOT

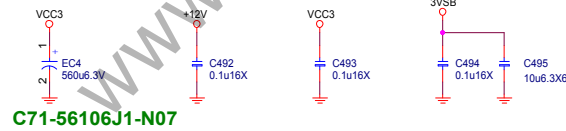
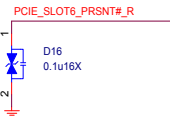


# PCI EXPRESS X8 SLOT

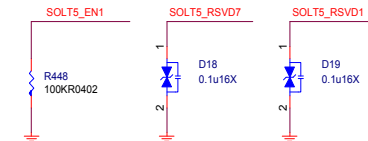
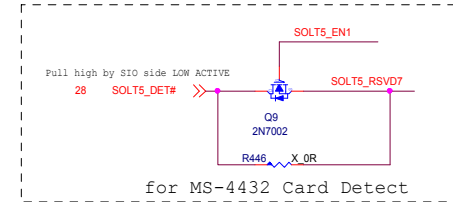
PCI\_E5



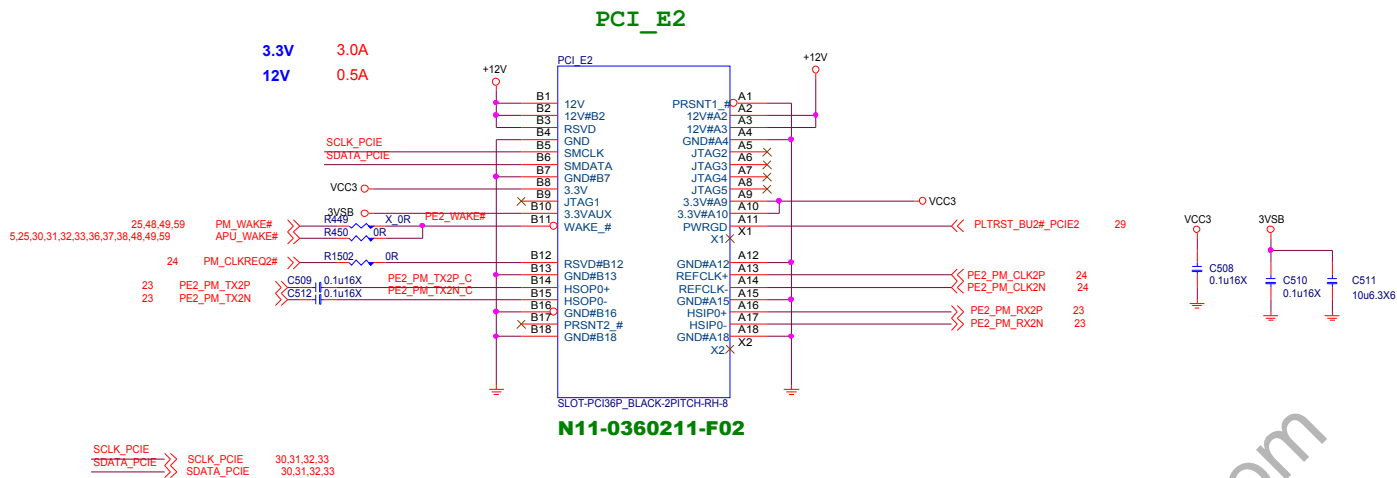
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C71-56106J1-N07



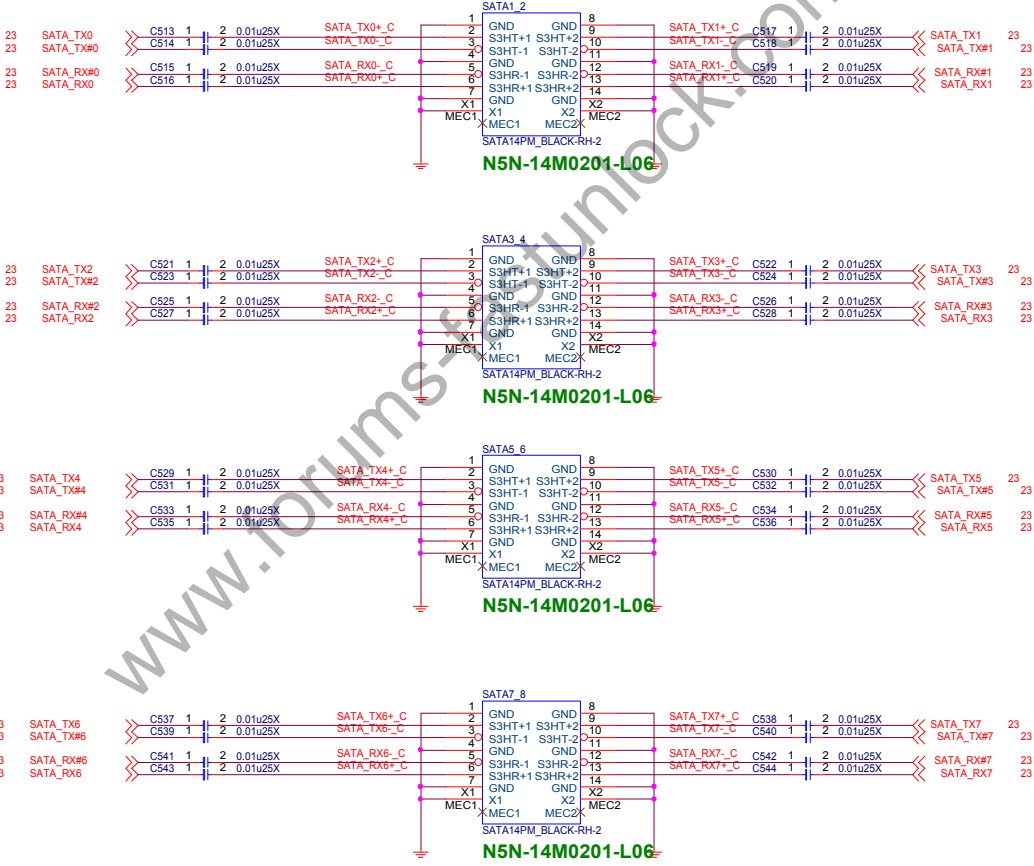
PCIEX1 12V 0.5A  
3.3V weak 375mA



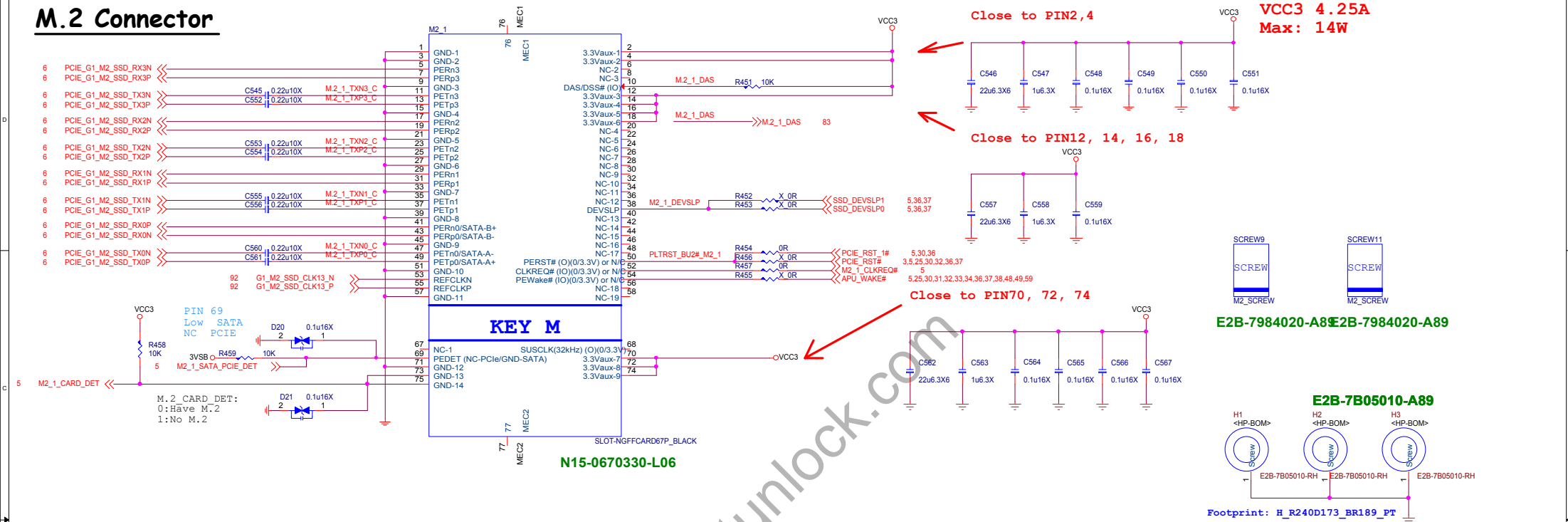
PCI Express X1 slot

+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

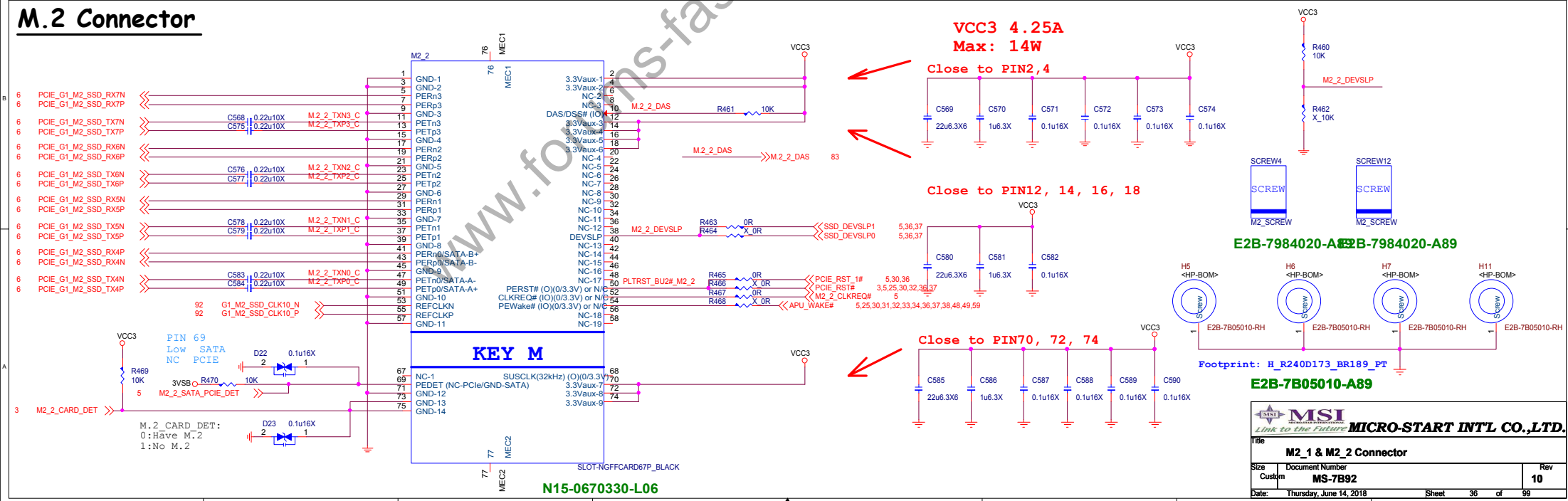
SATA Connector



## M.2 Connector

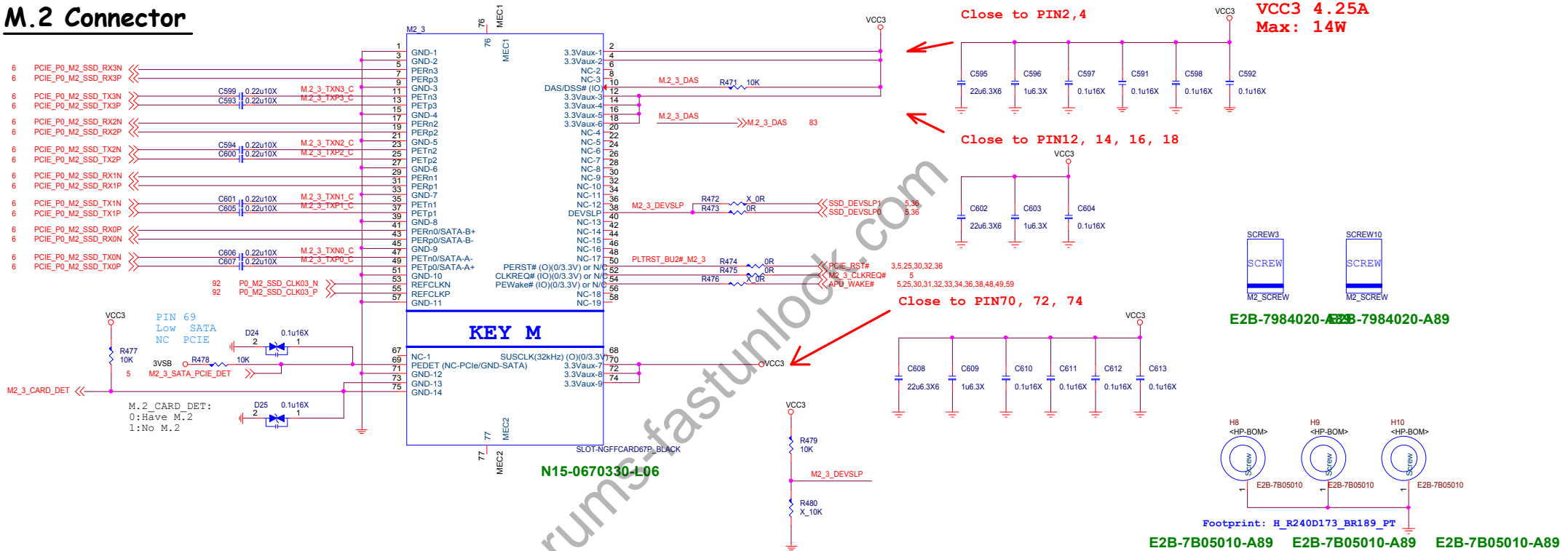


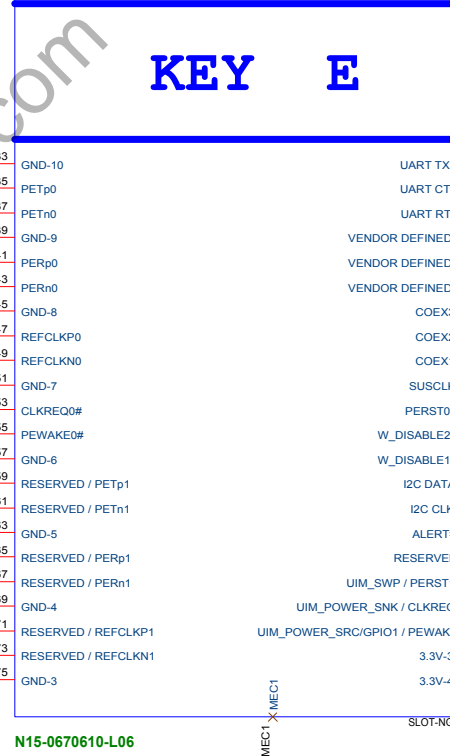
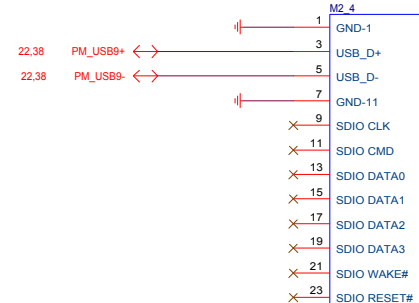
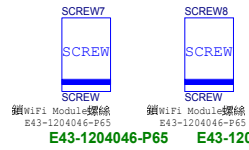
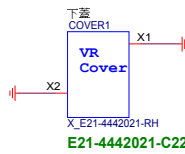
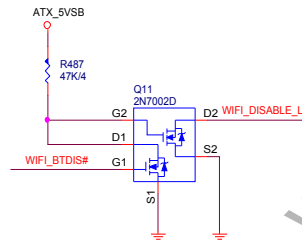
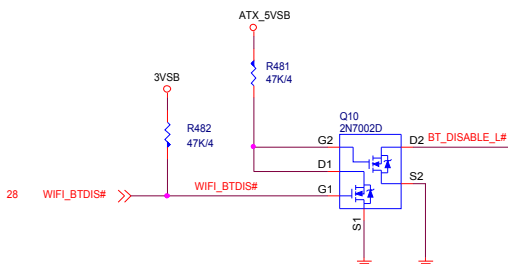
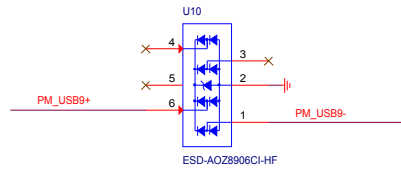
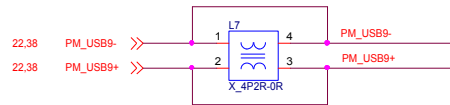
## M.2 Connector





## M.2 Connector



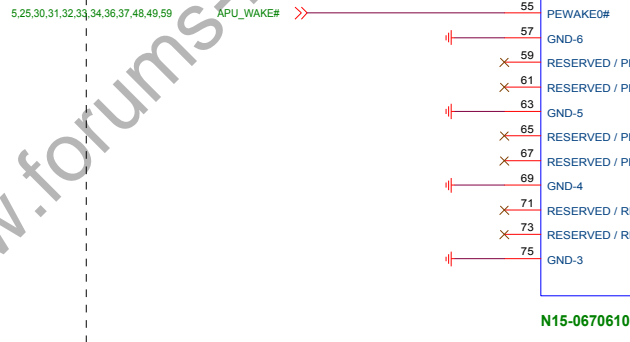


780mA

3VSB



KEY E



10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.  
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

**MSI**  
MICRO-START INTL CO.,LTD.

File: **M2\_4 WIFI+BT**

Size: **MS-7B92**

Date: Thursday, June 14, 2018

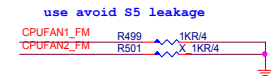
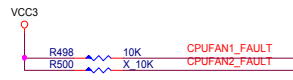
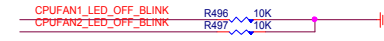
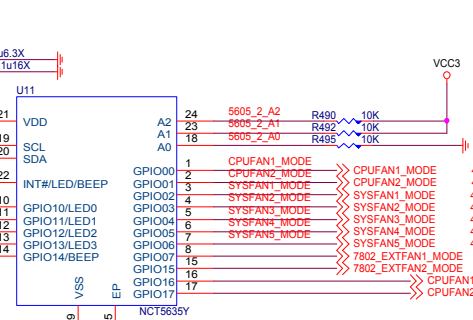
Sheet: 38 of 99

5,15,17,47,53,66,71,78,79,84,85,86,91,92  
5,15,17,47,53,66,71,78,79,84,85,86,91,92

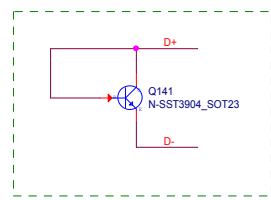
SPD\_SMBUS\_CLK  
SPD\_SMBUS\_DATA

40 CPUFAN1\_FAULT  
41 CPUFAN2\_FAULT  
40 CPUFAN1\_FM  
41 CPUFAN2\_FM

46 7802\_EXTFAN3\_MODE

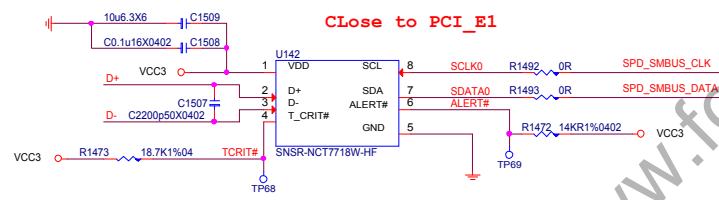


slave address :  
Write 4CH  
Read 4DH



Close to PCI\_E4

## NCT7718W



Layout notice:  
1. Put the CI 2200pF to close the NCT7718W.  
2. Add Ground Shielding For D+ and D- Traces.  
3. D+/D- Route Has to be Away From the High Noise Area.  
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

NCT7718W SM Bus address is 98h ( 1001100xb) Default: ALERT# Output Comparator Mode

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

**MSI**  
Micro-Start International Co., Ltd.

**MICRO-START INTL CO.,LTD.**

Title  
**CPU FAN Control NCT5635Y**

Size  
 Custom

Document Number  
**MS-7B92**

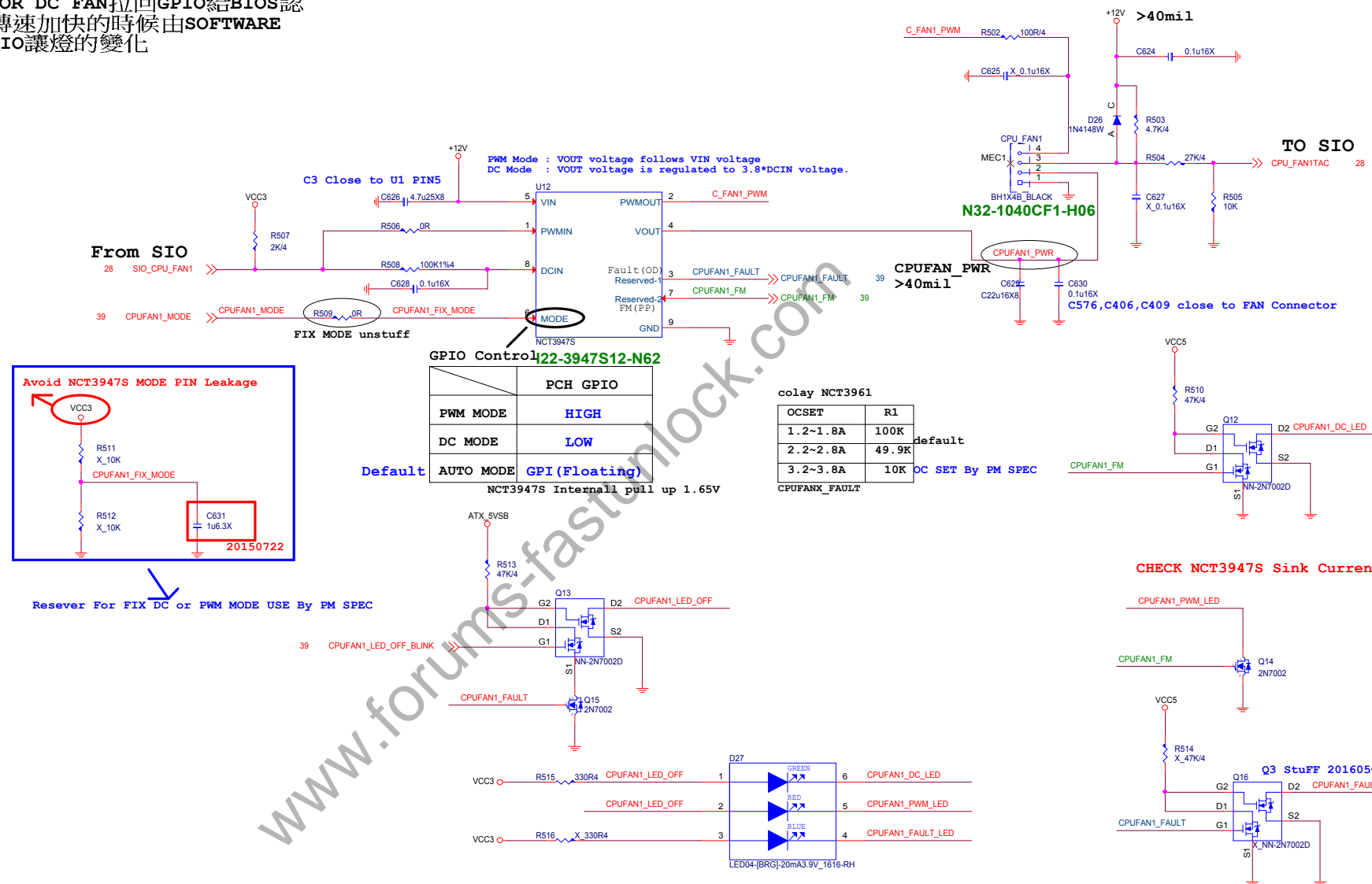
Rev  
**10**

Date: Thursday, June 14, 2018

Sheet 39 of 99

# TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

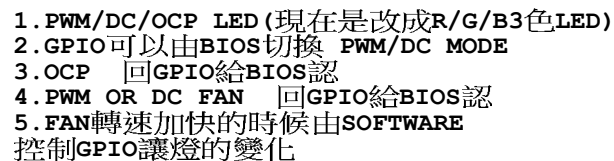
1. PWM/DC/OC LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCP拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化



1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
2. FAULT : USE FAULT PIN Triger OVT/OC Protection, LOW Atcive (Reserve NEW IC)
3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

**PM SPEC更新成TYPE-K , 只改BOM**

- PM SPEC更新成TYPE-K , 只改BOM**



Resever For FIX DC or PWM MODE USE By PM SPEC

GPIO Control	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPIO(Floating)

```
colay NCT3961
```

OCSET	R1
1.2~1.8A	100K
2.2~2.8A	49.9K
3.2~3.8A	10K

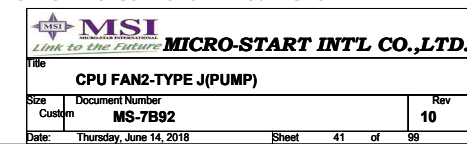
OC SET

CPUFANX FAULT

OC SET By PM SPEC

CHECK NCT3947S Sink Current

CHECK NCT3947S Sink Current



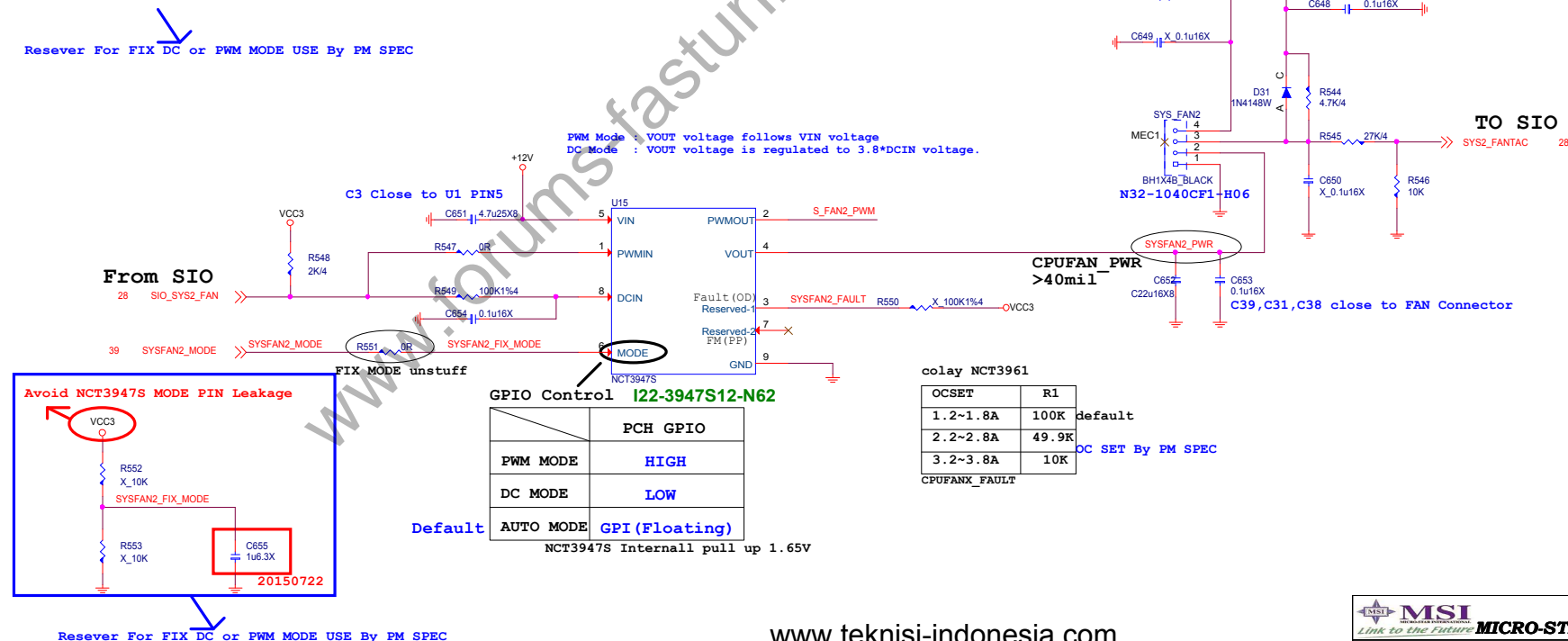
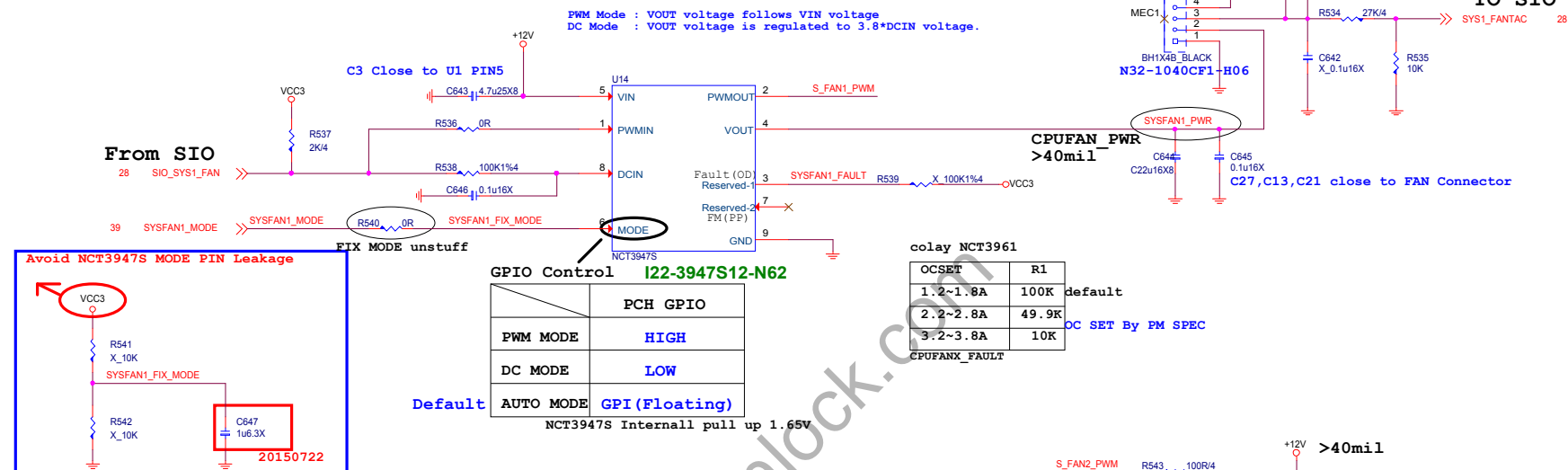
- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN) FAN\_OCP\_LED(紅)  
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)  
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

RGB  
D0C-040S400-H91

20161024 Update  
DC\_FAN\_LED(綠)  
PWM\_FAN\_LED(藍)  
FAN\_OCP\_LED(紅)

# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

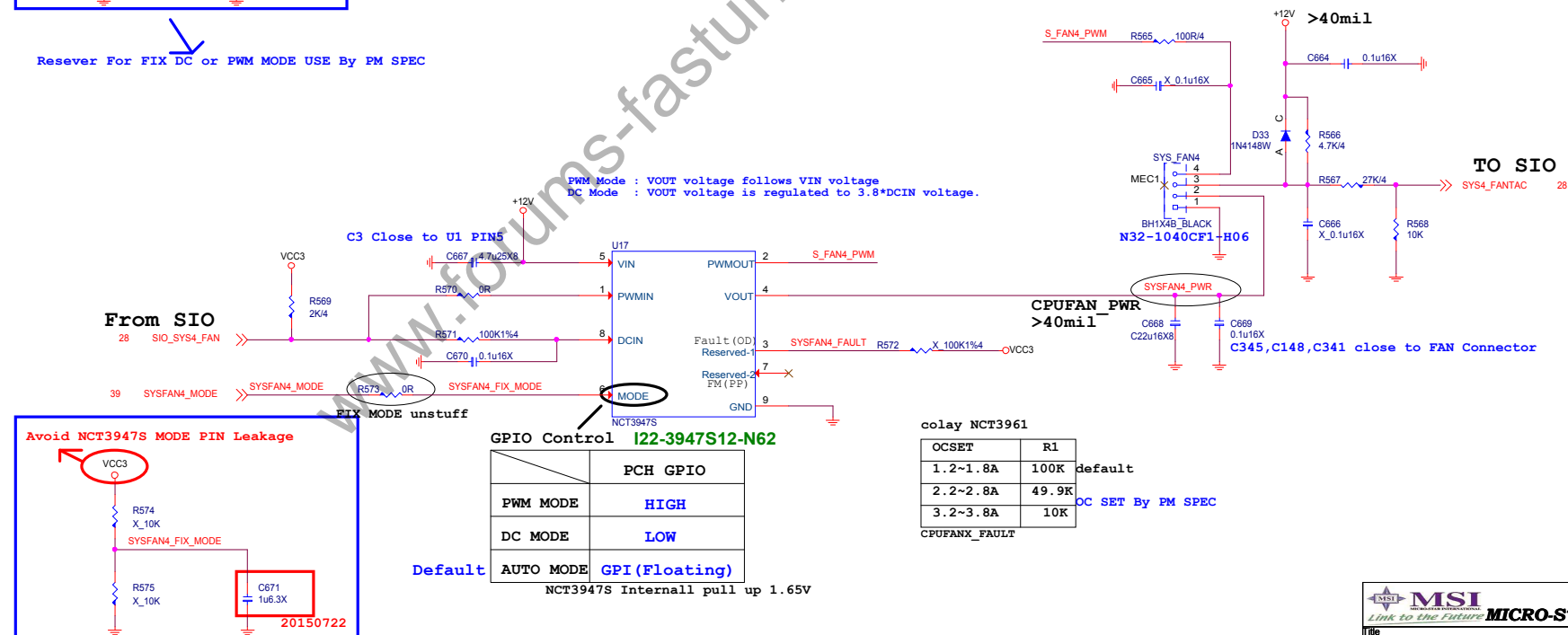
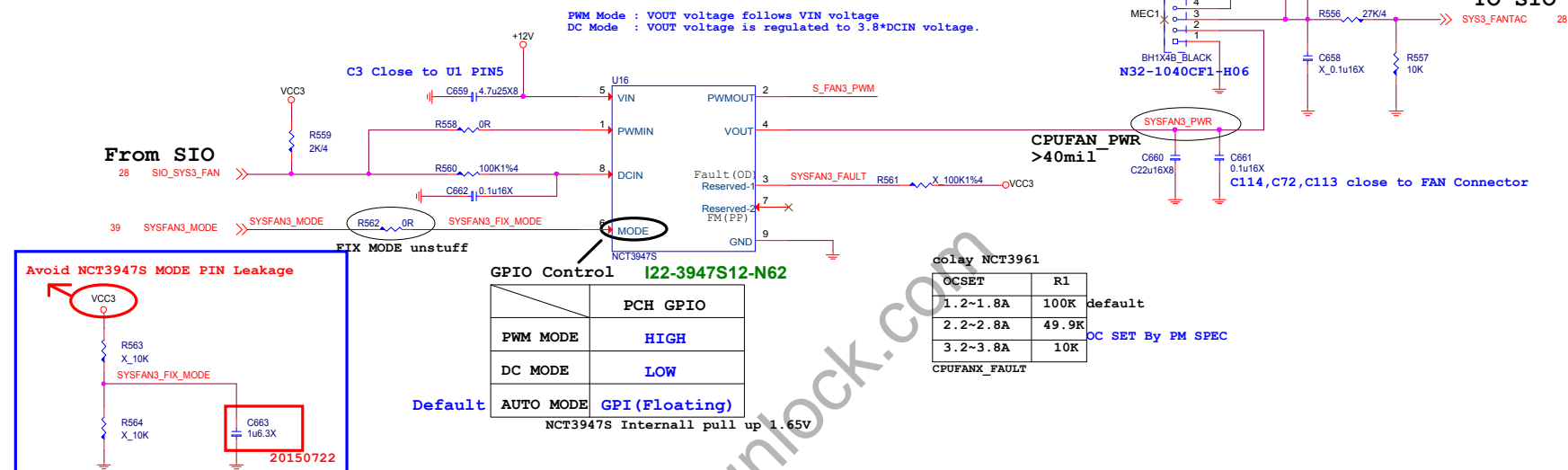
1. Mode GPIO BIOS can switch PWM/DC Mode
2. FM:BIOS can read FAN PWM/DC Mode



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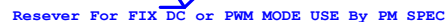
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

## 1. Mode GPIO BIOS can switch PWM/DC Mode

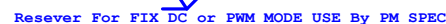




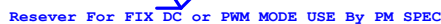
## 1. Mode GPIO BIOS can switch PWM/DC Mode

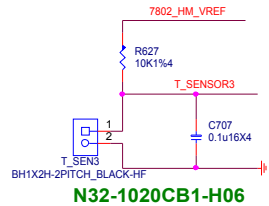
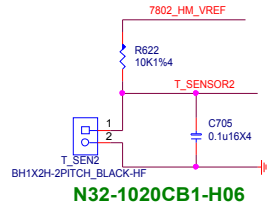
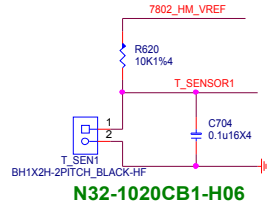


## 1. Mode GPIO BIOS can switch PWM/DC Mode



## 1. Mode GPIO BIOS can switch PWM/DC Mode





46 7802\_EXTSYS3\_FAN <<

T\_SENSOR3

T\_SENSOR2

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

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T\_SENSOR1

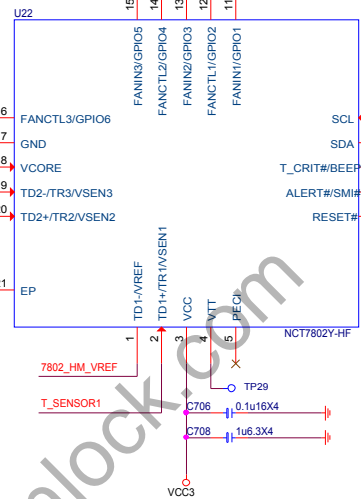
T\_SENSOR1

T\_SENSOR1

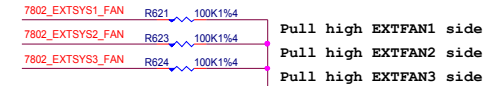
T\_SENSOR1

T\_SENSOR1

T\_SENSOR1

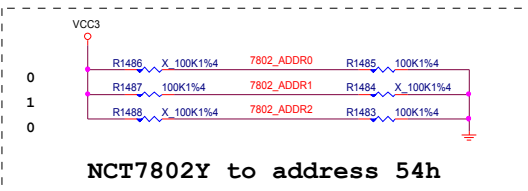


PUSH-PULL

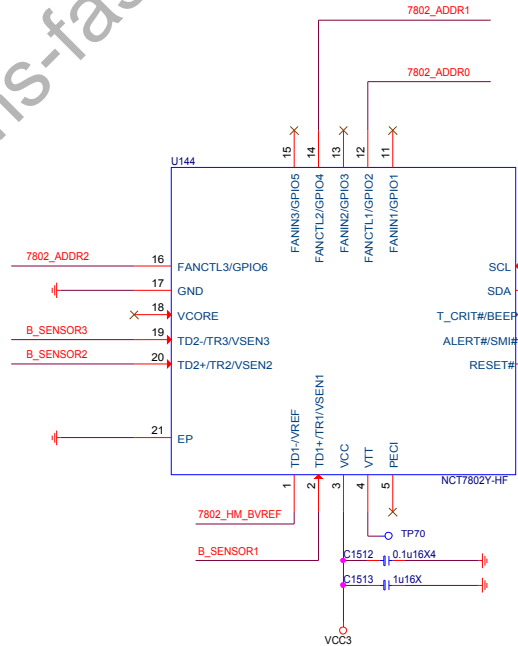


NCT7802Y to address 50h

Sense T\_SEN1 control EXTFAN1  
Sense T\_SEN2 control EXTFAN2  
Sense T\_SEN3 control EXTFAN3



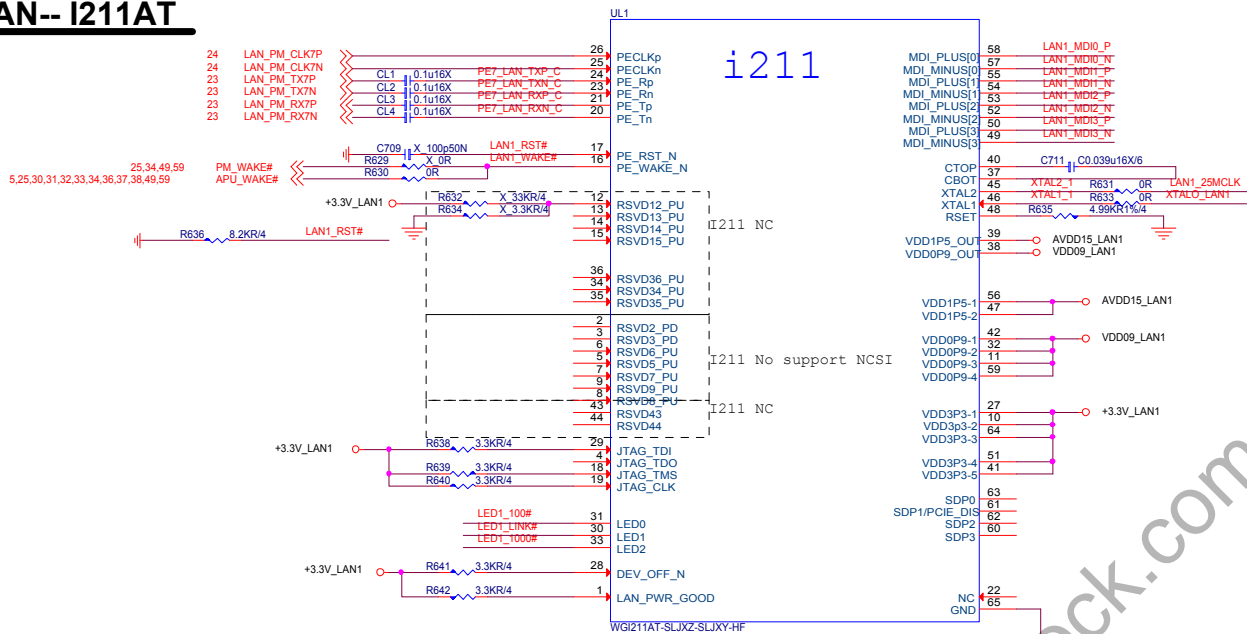
NCT7802Y to address 54h



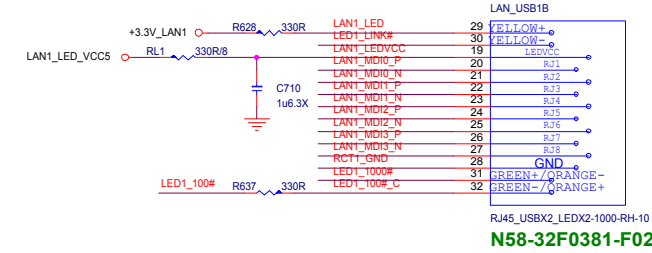
NCT7802\_B\_SMBCLK SPD\_SMBUS\_CLK  
NCT7802\_B\_SMBDAT SPD\_SMBUS\_DATA

# LAN-- I211AT

## LAN Connector

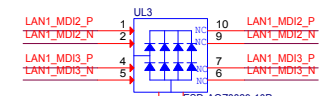
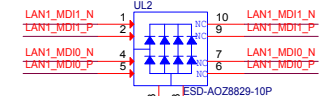
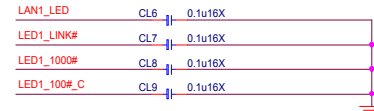
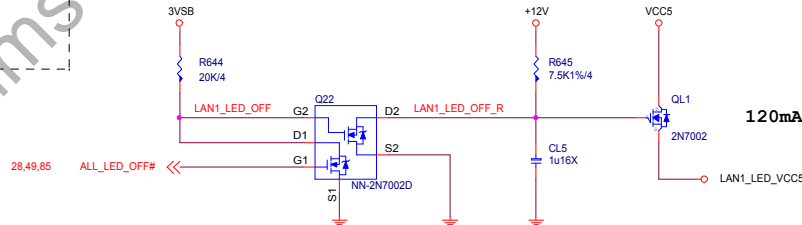
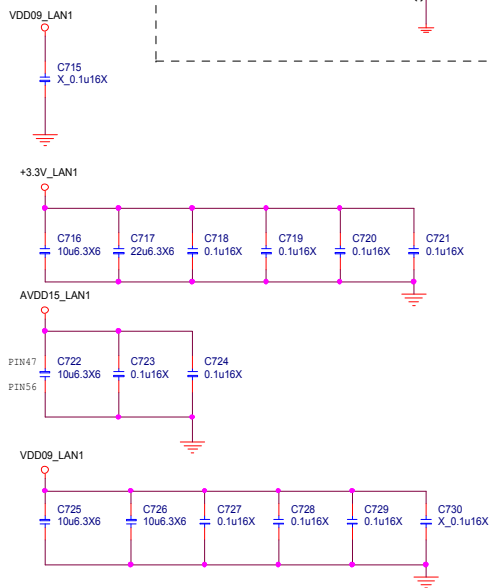
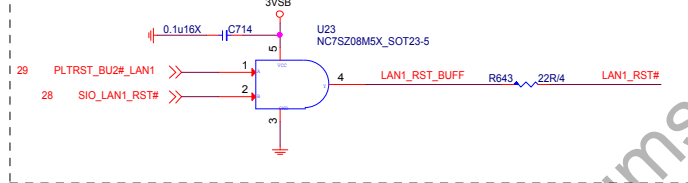


## LAN+USB1



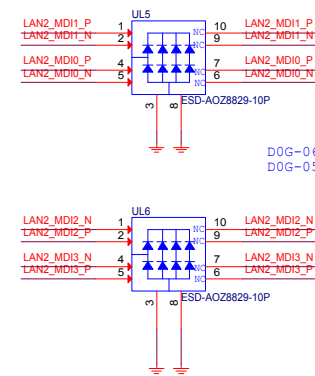
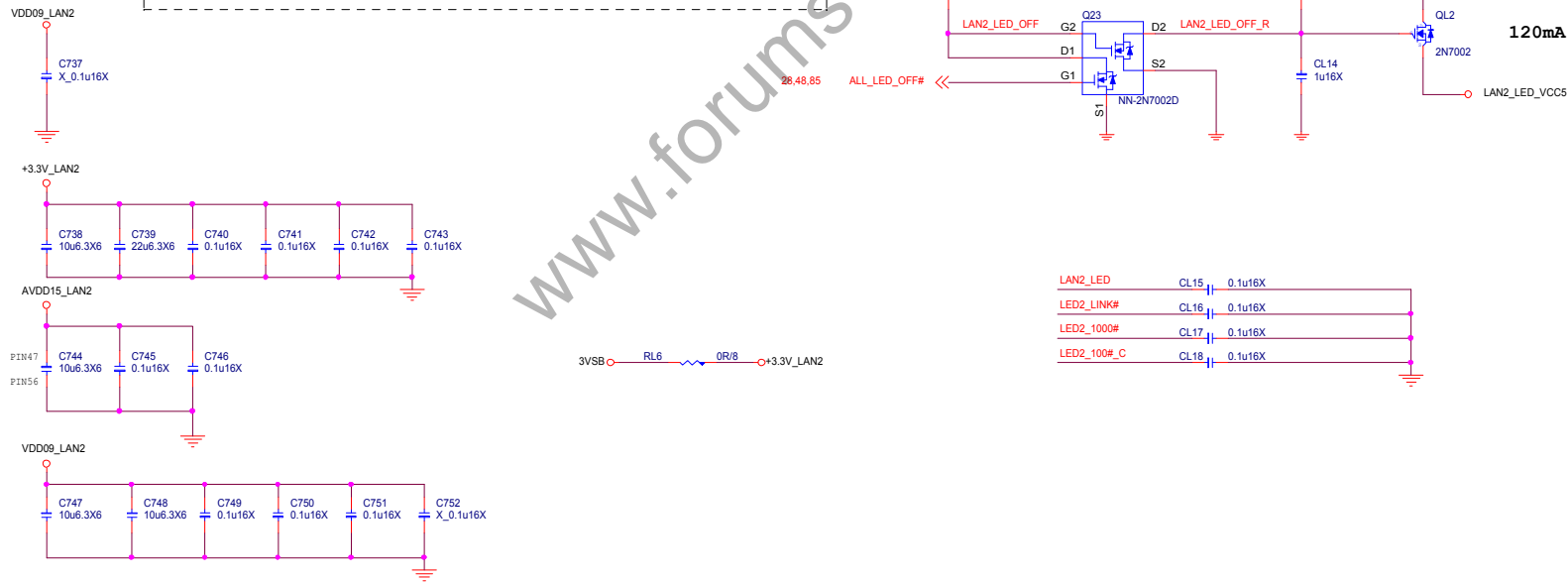
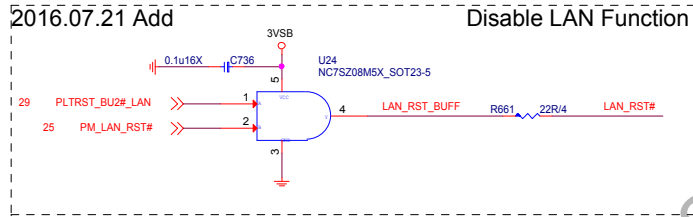
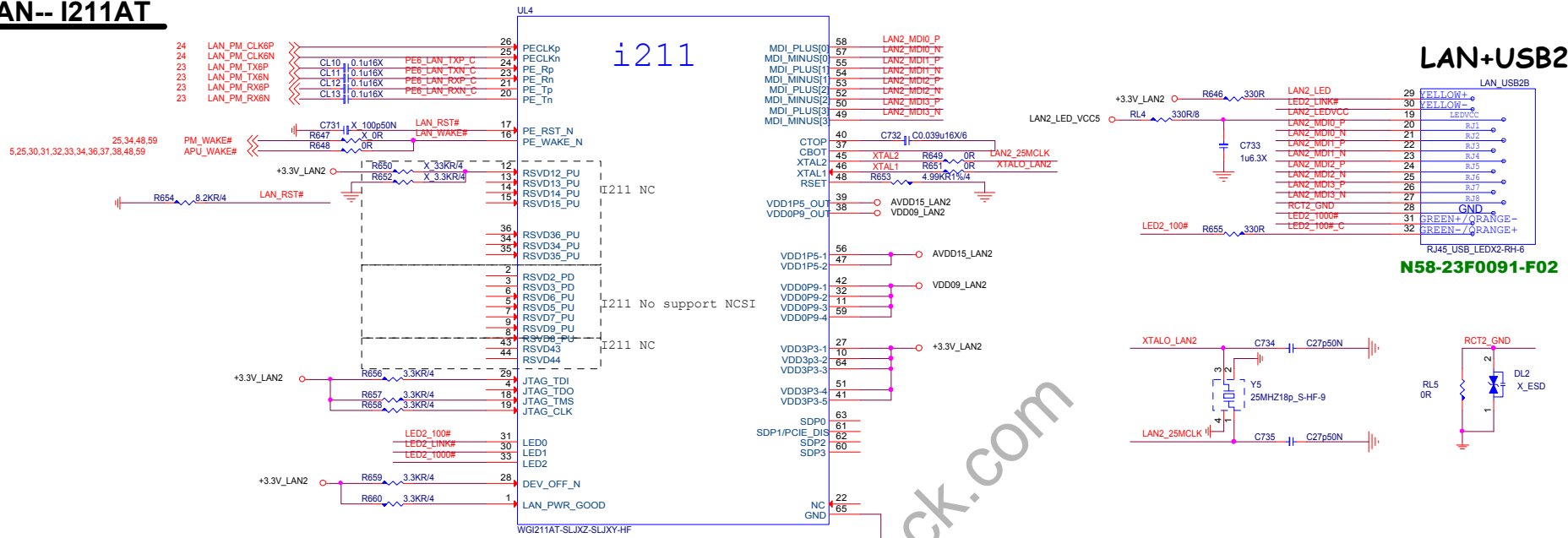
2016.07.21 Add

Disable LAN Function



File			LAN1-Intel I211AT
Size	Document Number	Rev	
Custom	MS-7892	10	
Date:	Thursday, June 14, 2018	Sheet	48 of 99

**LAN-- I211AT**



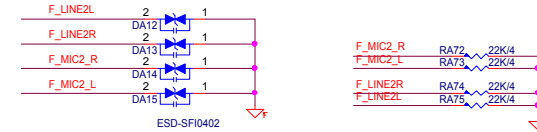
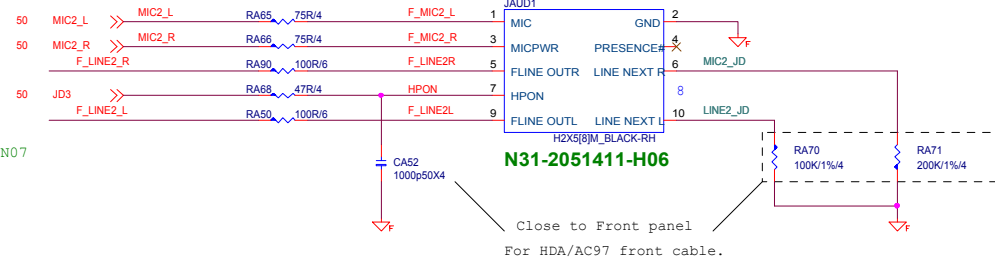
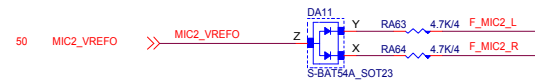
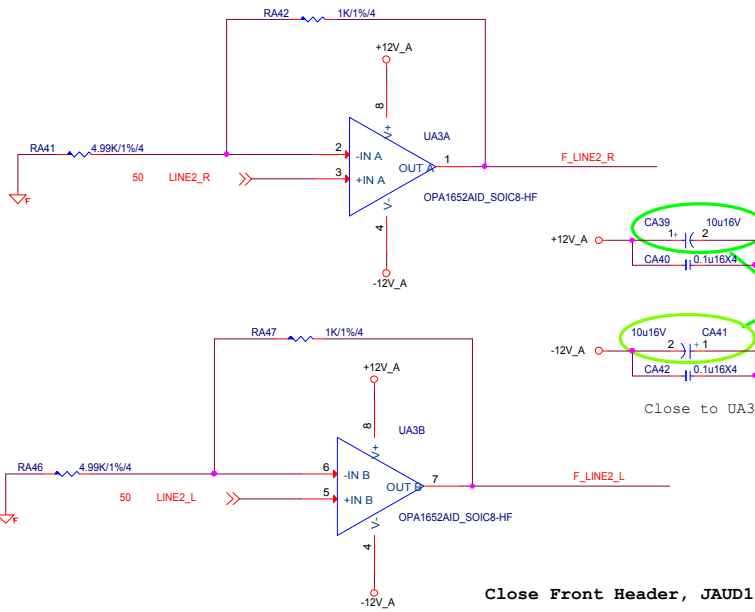




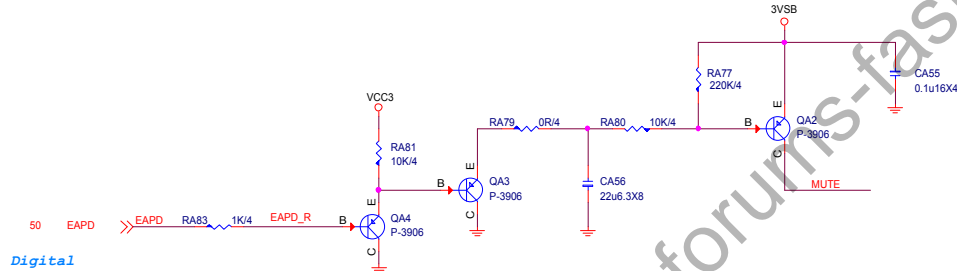
Removed Ess9023

Analong SW1

Analong SW2



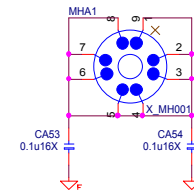
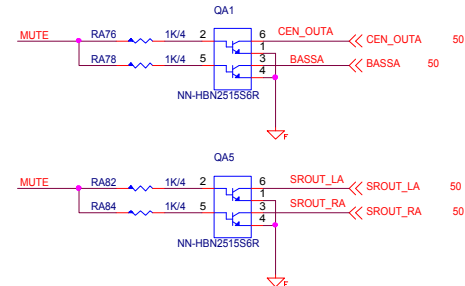
### Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out)



Analog

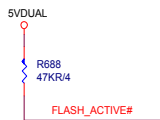
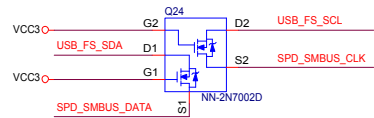
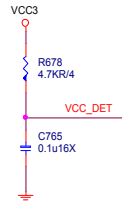
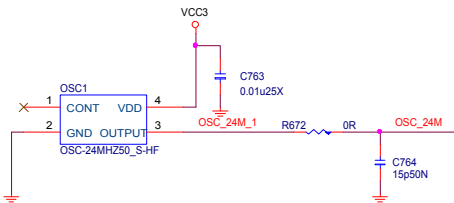


(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)



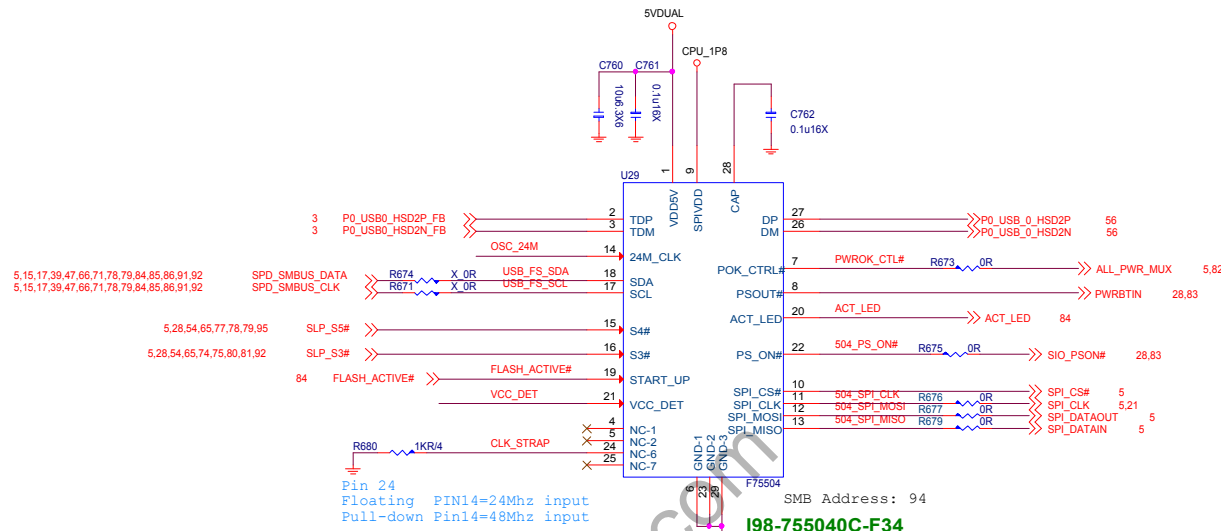
# USB Flash BIOS

Host USB connector

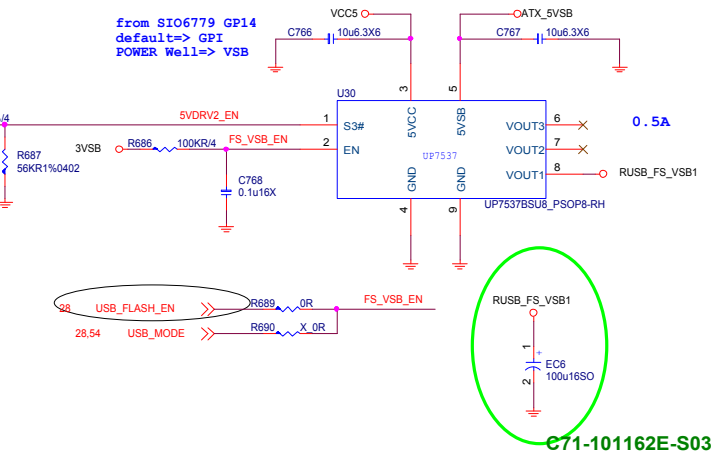


Reserved for when F75501 Hotkey device fail use

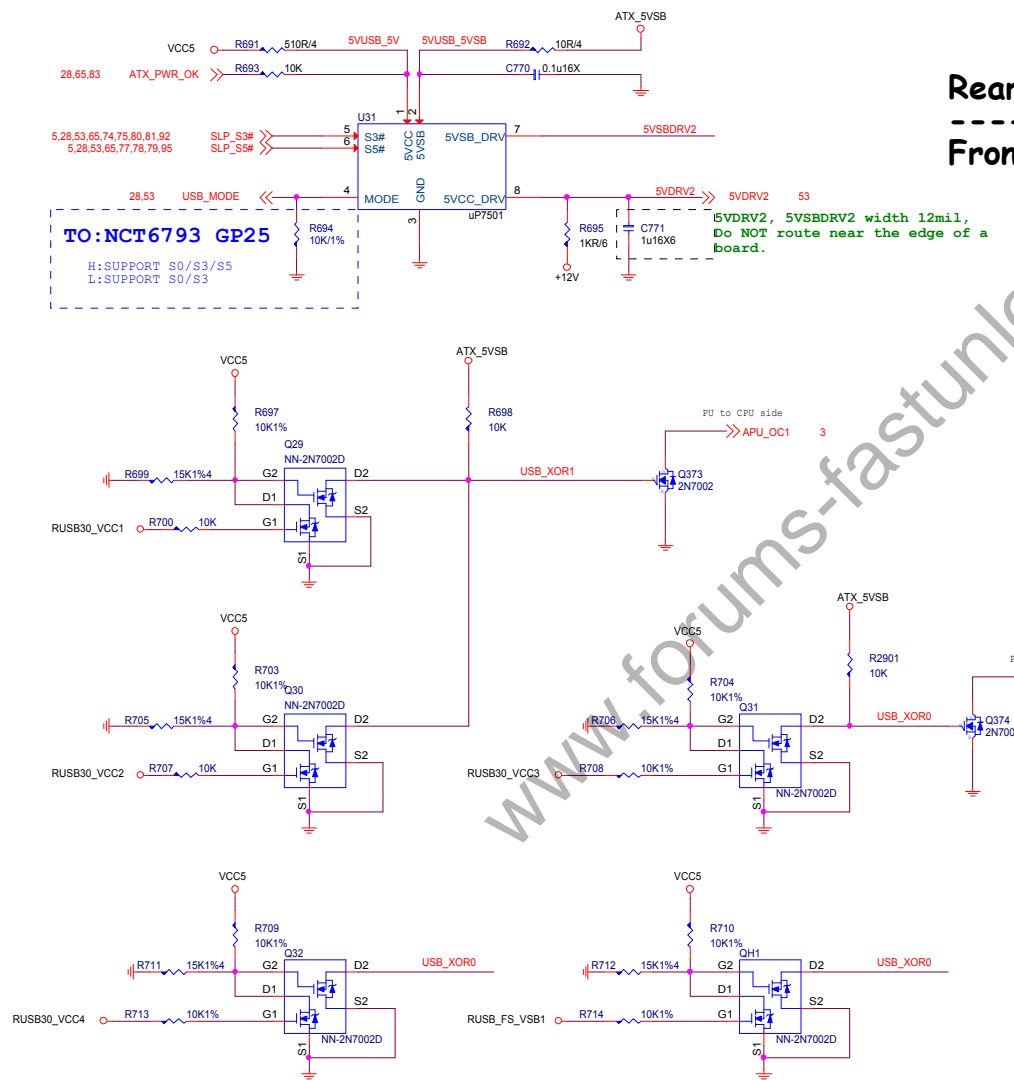
\* All close to Front IO side



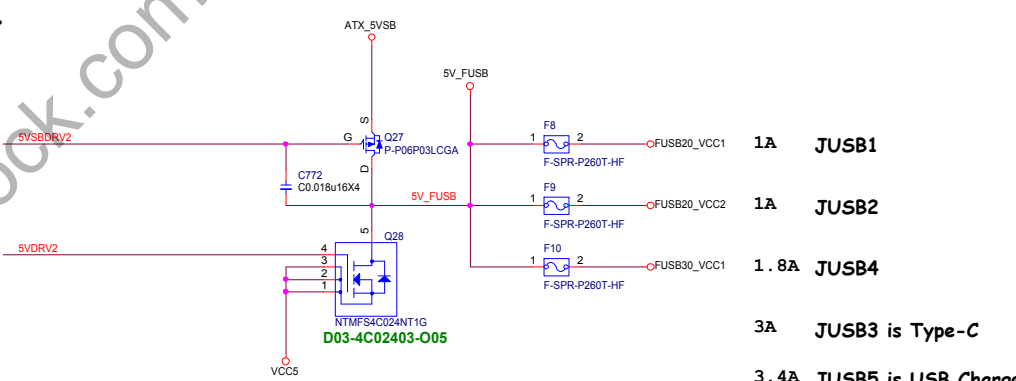
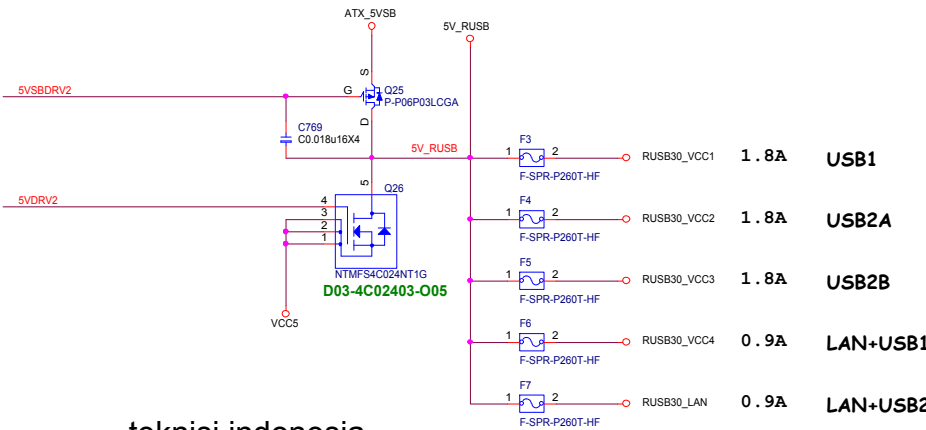
## REAR Flash BIOS USB PORT



USB Power

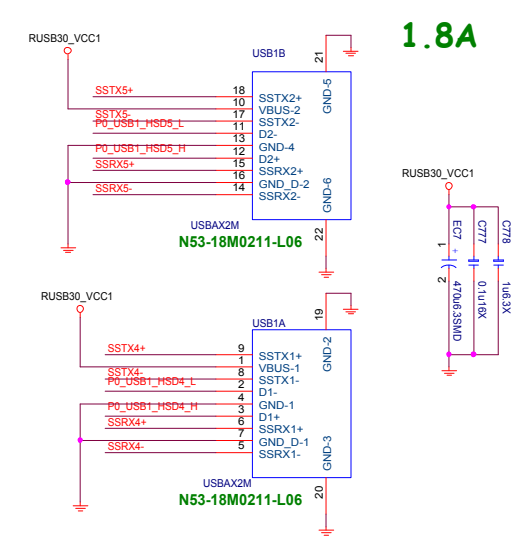
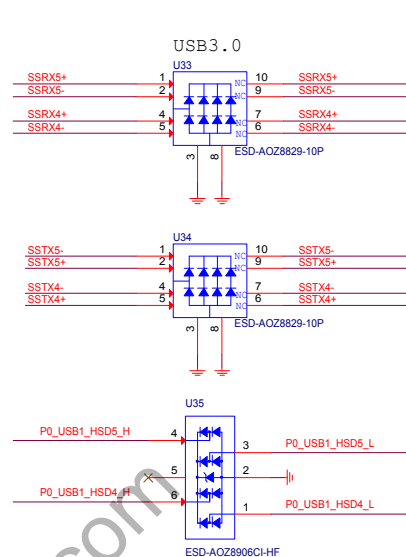
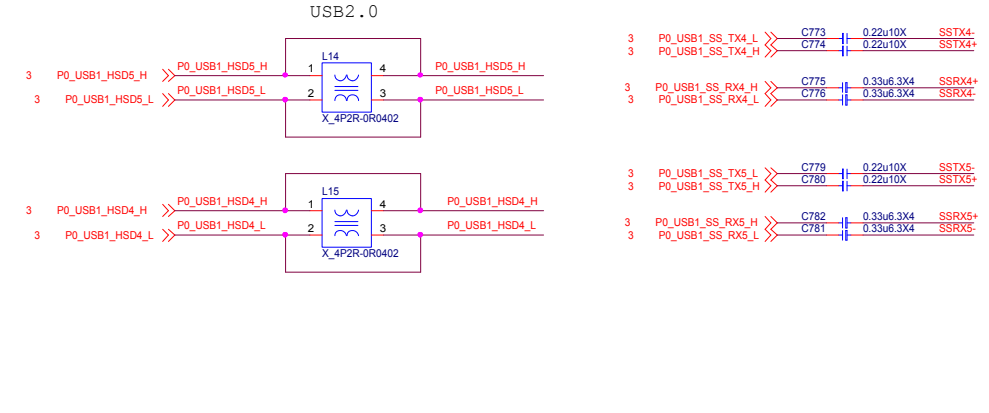


Rear  
Front

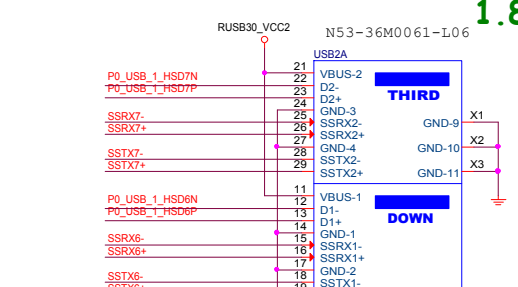
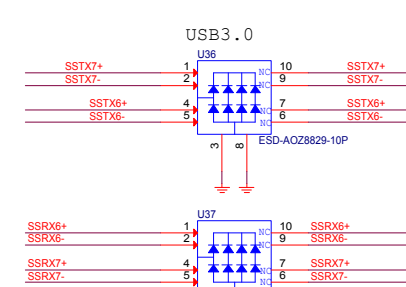
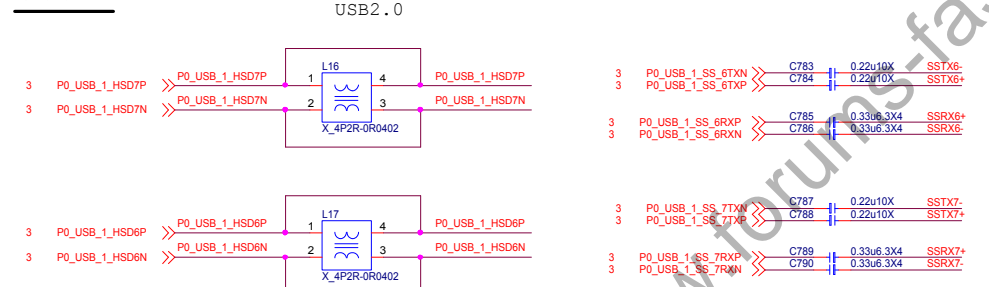


	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

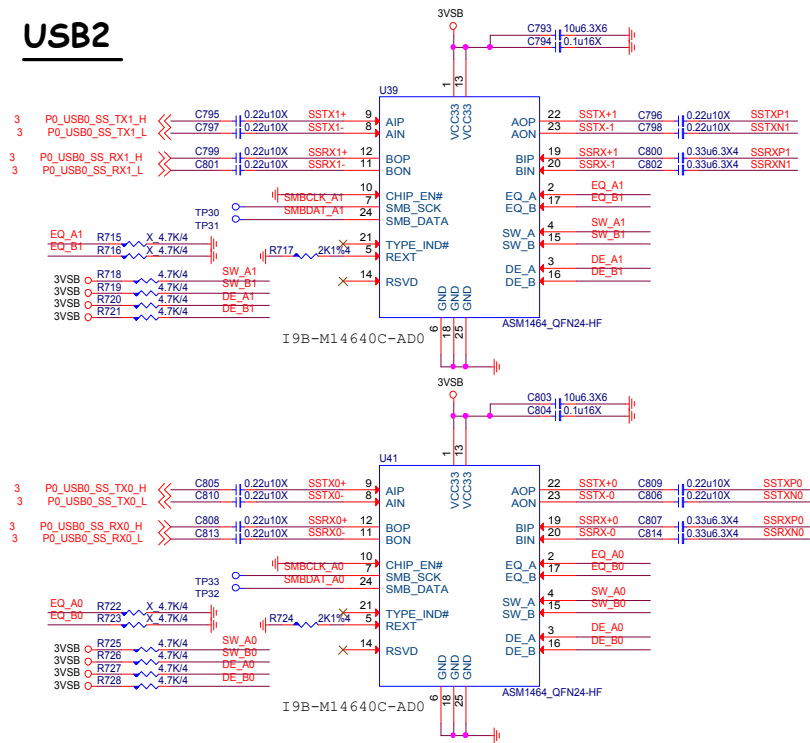
USB1



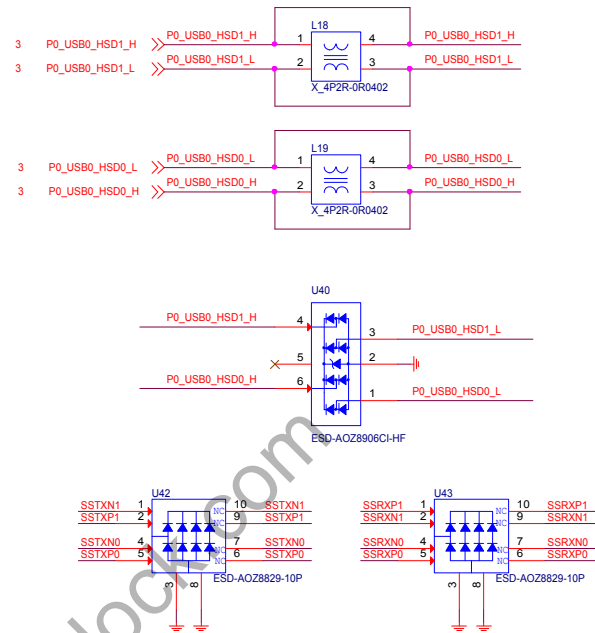
USB2



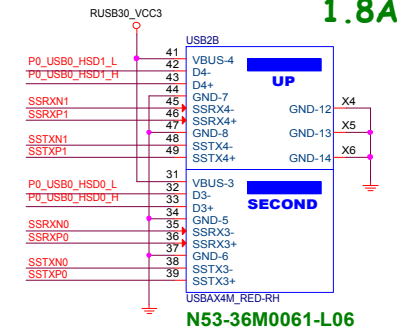
## USB2



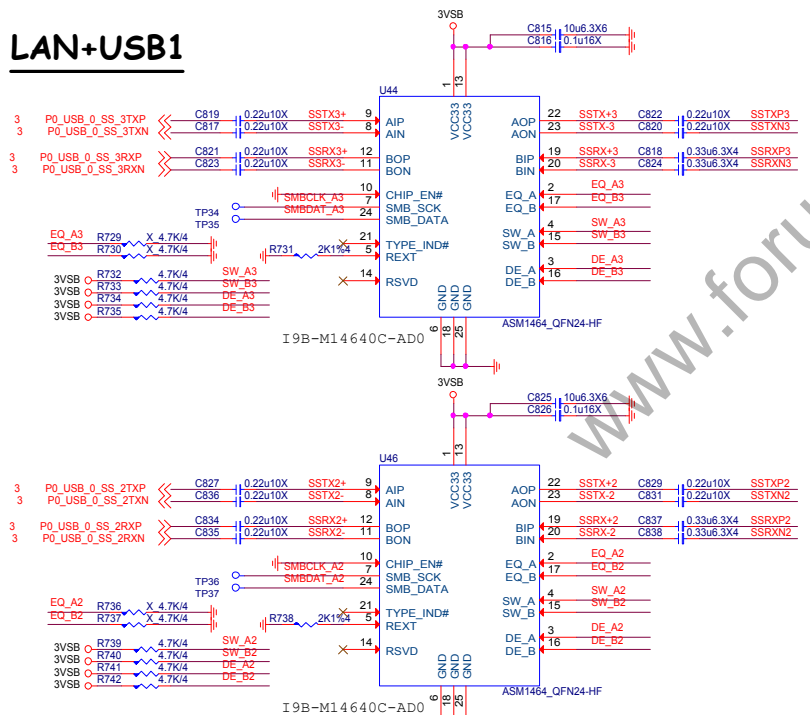
## USB2.0



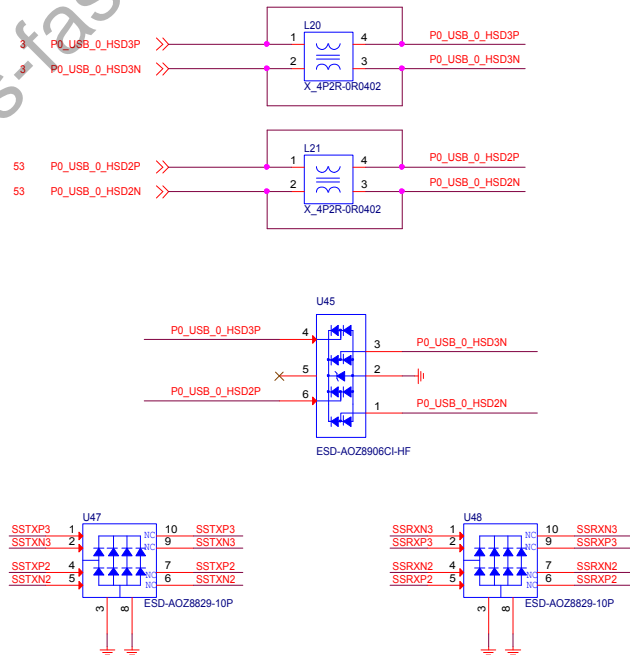
## 1.8A



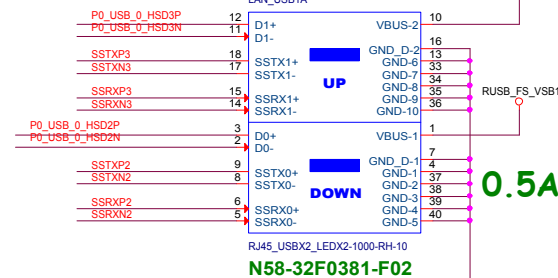
## LAN+USB1



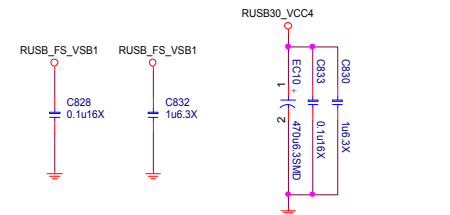
## USB2.0

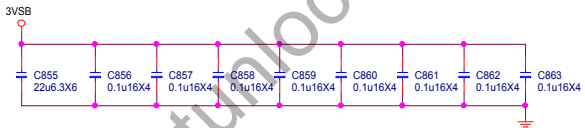
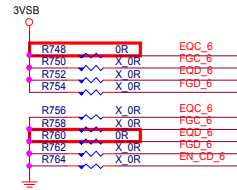
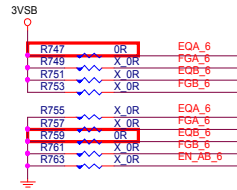
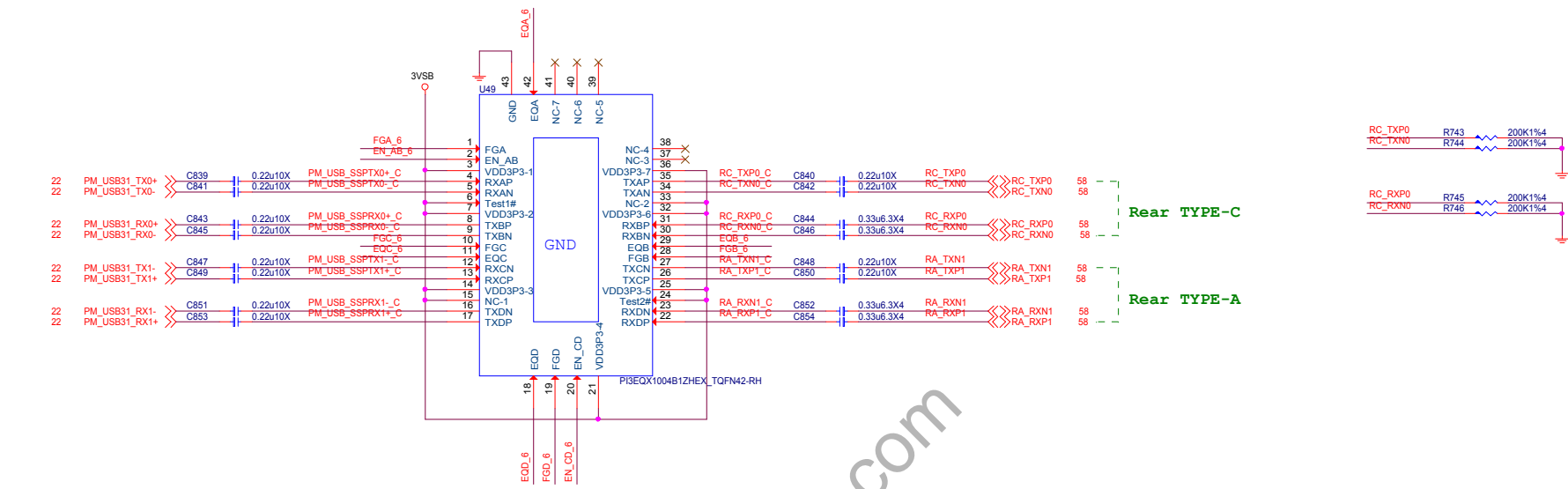


## 0.9A



## 0.5A





EQ	dB	
0	12.4	0 to GND
R	8	68K to GND
F	10.6	NC
1	14.6	0 to VDD

FG	dB	
0	-1.6	0 to GND
R	-0.5	68K to GND
F	1.0	NC
1	2.7	0 to VDD

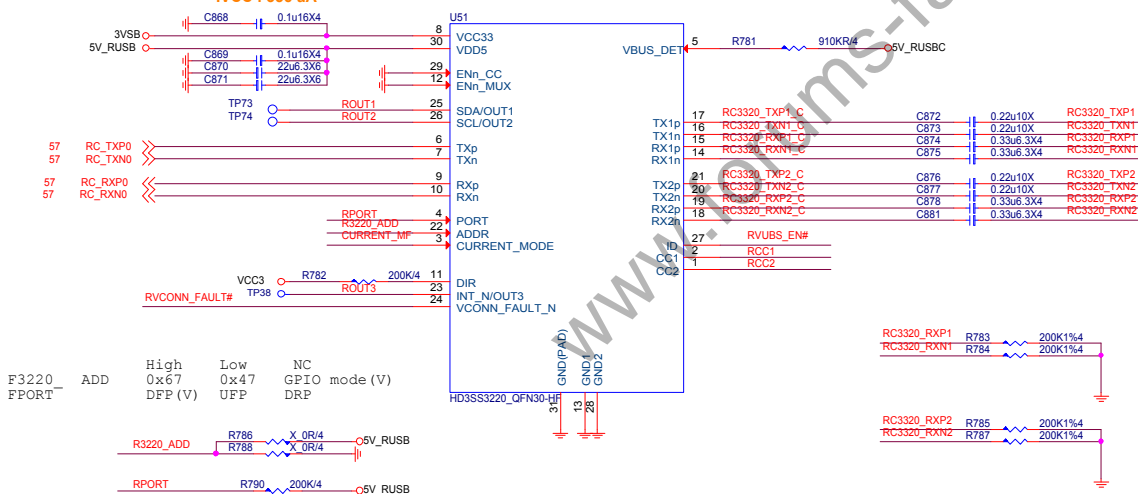


VBUS EN

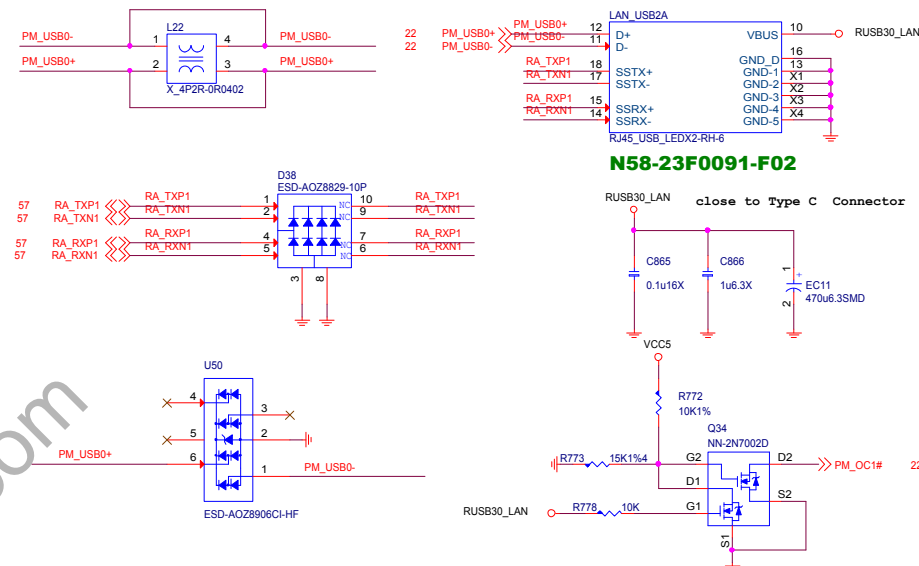
Current Mode

## USB Type-C MUX with Configuration Channel (CC)

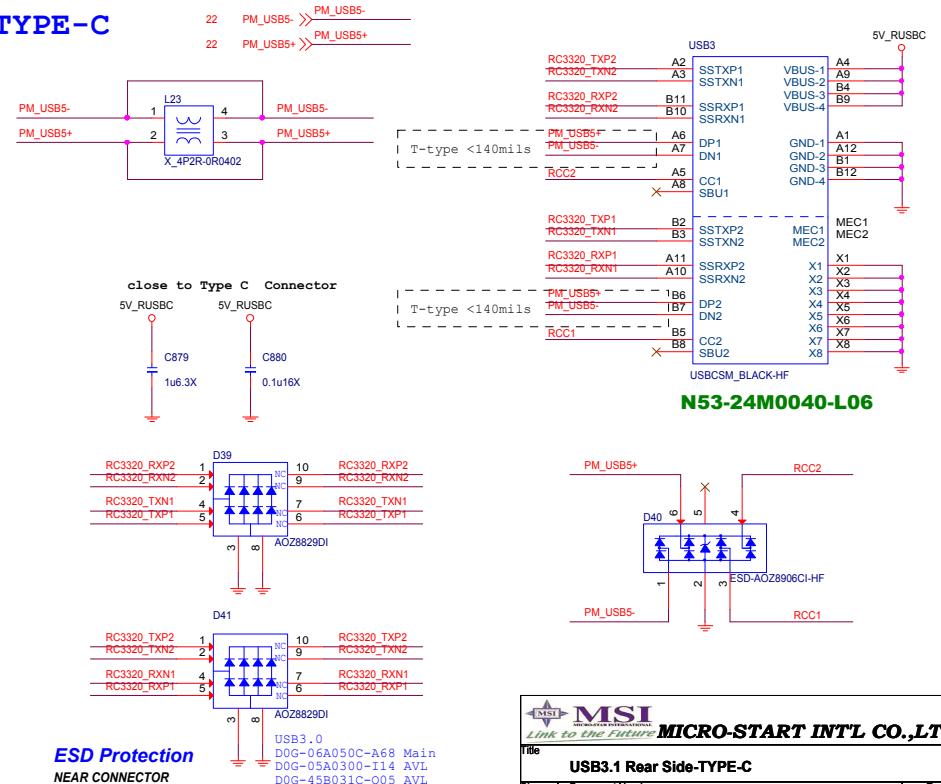
IVCC : 356 uA



## TYPE-A



## TYPE-C



## LAN+USB2

N58-23F0091-F02

close to Type C Connector

N53-24M0040-L06

ESD Protection  
NEAR CONNECTOR

USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL  
D0G-45B031C-005 AVL

MSI Link to the Future		MICRO-START INTL CO.,LTD.	
Title USB3.1 Rear Side-TYPE-C			
Size Custom	Document Number MS-7B92	Rev 10	
Date Thursday, June 14, 2018	Sheet 58	of 99	

Use pure PCIE must provide CLK

Minimum gap should be greater of  
>15mil with other signal.

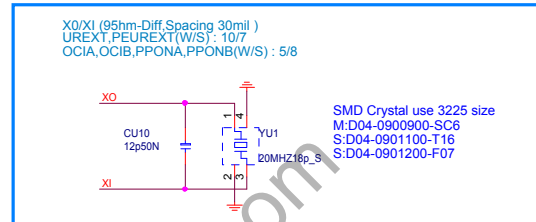
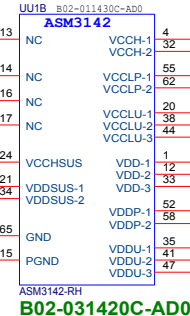
Front side USB3.1 TYPE C

Layout Guide:

- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

Power Consumption

	3.3V	3.3VSUS	2.5V	1.1V	1.1VSUS	Unit
ASM3142	TBD	TBD	TBD	TBD	TBD	mA
ASM2142	4	9	220	470	10	mA



ASM3142  
B02-031420C-AD0

2016.07.21 Add

Disable ASM1142 Function

ASM3142 1.1v Core Power

ASM3142 1.1v Suspend Power

ASM3142 2.5v Analog Power

EEPROM

M31-25L1022-M24

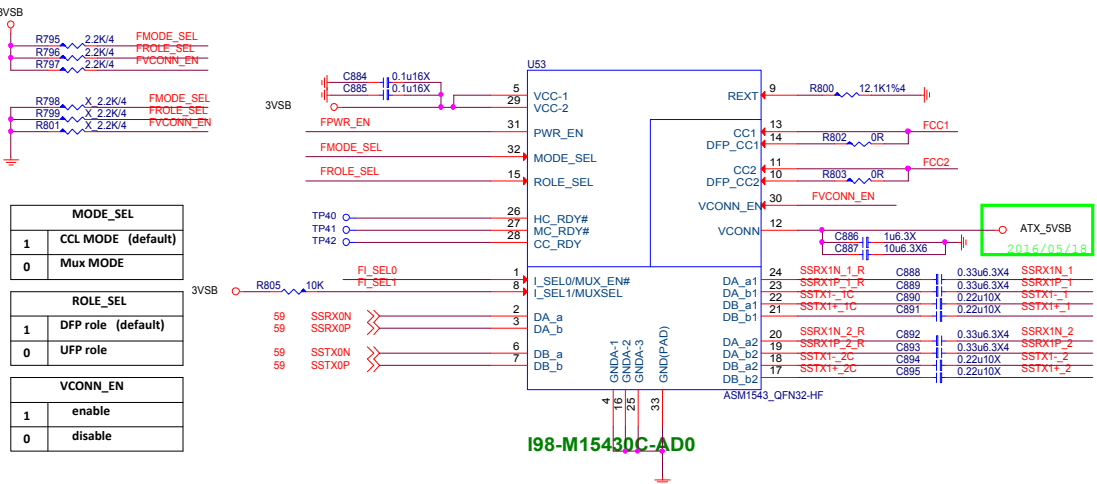
M: M31-25L1022-M24 (1M)  
S: M31-25X2023-W03 (2M)

MSI  
Link to the Future  
MICRO-START INTL CO.,LTD.

Title USB3.1 ASM1142-1		
Size Custom	Document Number MS-7B92	Rev 10
Date Thursday, June 14, 2018	Sheet 59 of 99	

# ASM3142 USB 3.1-Front Type-C

## USB Type-C MUX with Configuration Channel (CC)



EQA/B are the selection pins for the equalization selection

EQA/B	Equalizer setting (dB)	
	@2.5GHz	@5GHz
0	5.1	10.9
R	1.9	6.7
F	3.5	8.9 (Default)
1	6.8	13.1

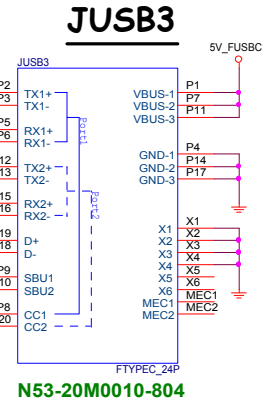
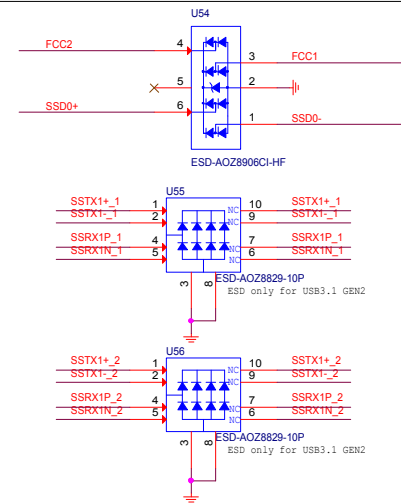
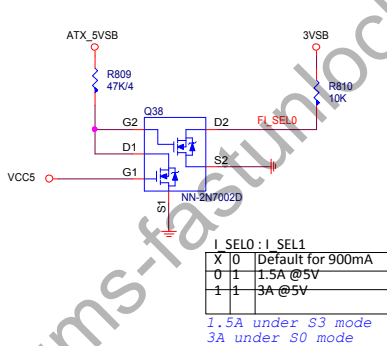
**Flat Gain Setting:**  
FGA/B are the selection bits for the DC gain

FGA/B	Flat Gain Settings	
	dB	
0	-3	
R	-1.5	
F	0 (Default)	
1	+2	

**-1dB compression point linear Swing Setting:**  
SWA/B are the selection bits for the output linear swing setting

SWA/B	Output Linear Swing Settings	
	mVppd	
0	800	
R	1200	
F	1000 (Default)	
1	1100	

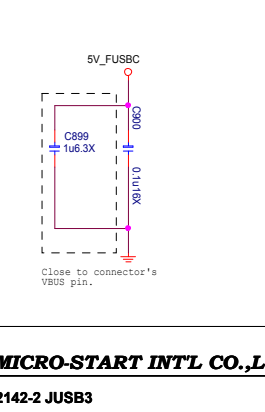
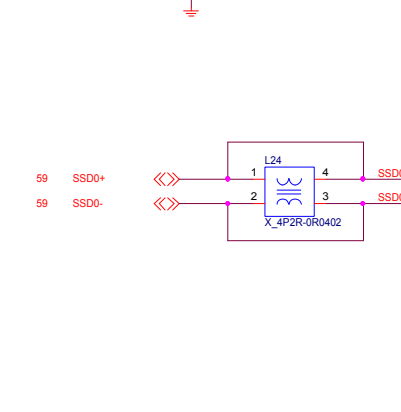
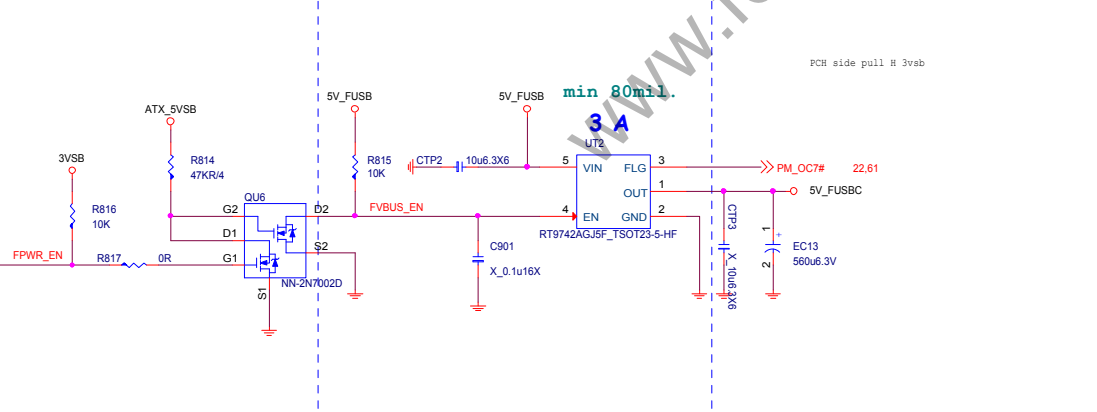
### Current Mode



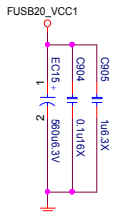
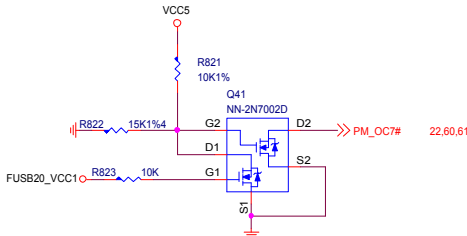
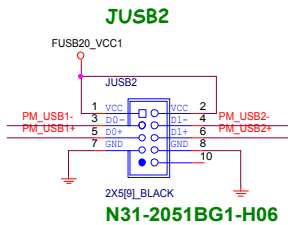
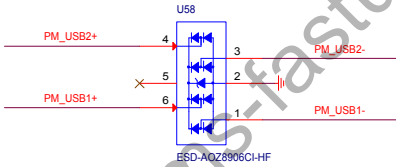
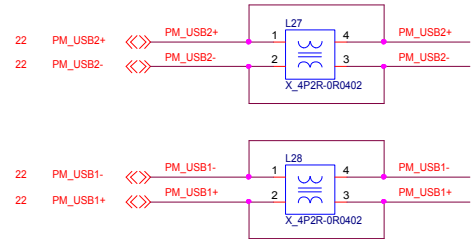
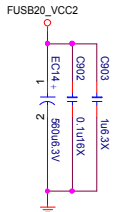
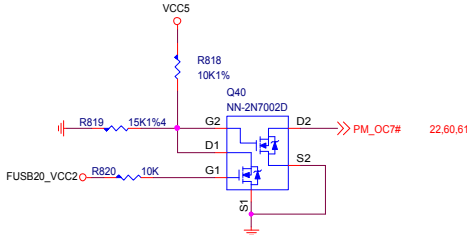
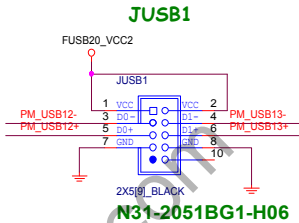
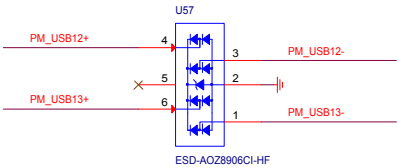
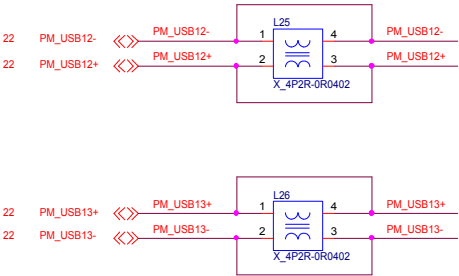
### VCOM OC#

### VBUS EN

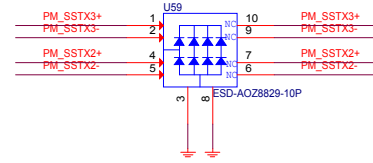
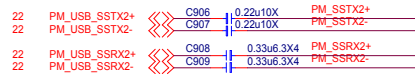
### VBUS OC#



JUSB1+JUAB2

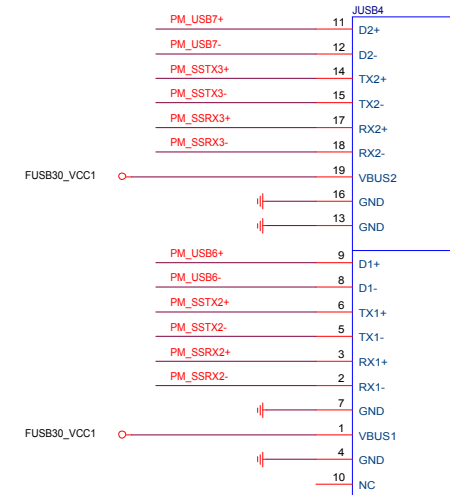
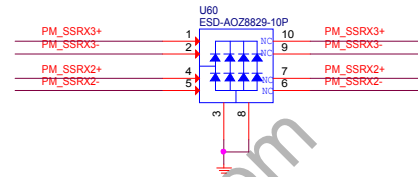
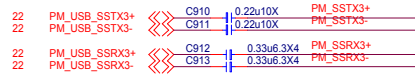


# USB 3.0-JUSB4

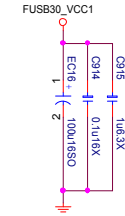
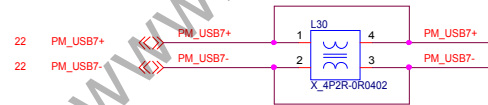
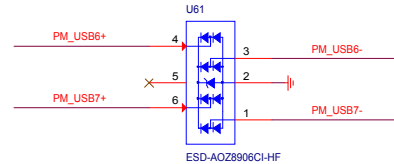
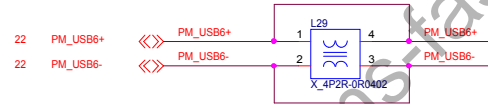
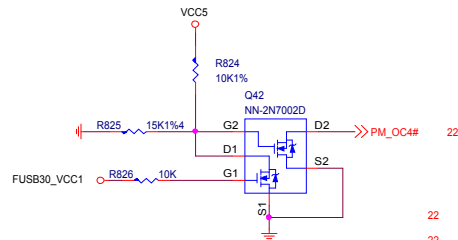


JUSB4

1.8A



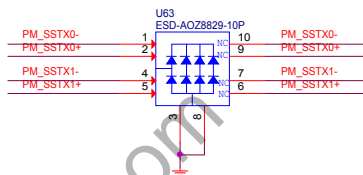
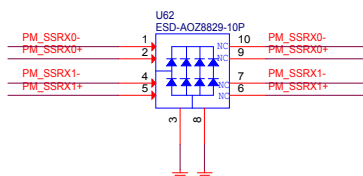
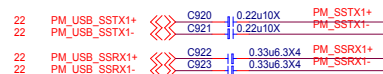
EX10 CONNECTOR  
BH2X10(20#-2PITCH\_BLACK-RH-4  
N32-2101731-AO3



# USB 3.0-JUSB5 With Charge(BC1.2)

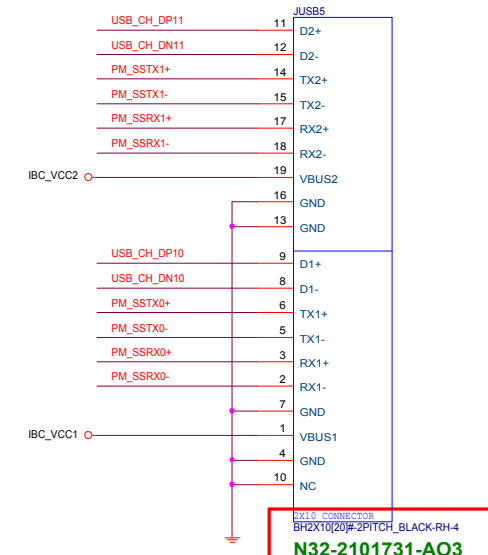
JUSB5

1.7A+1.7A

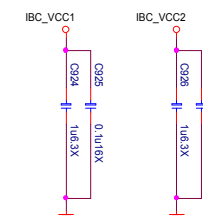
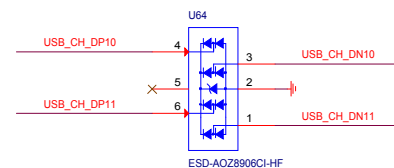
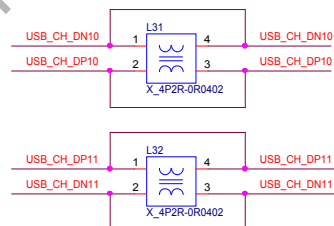
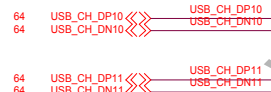


USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL

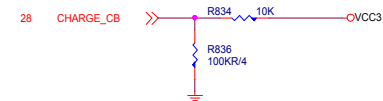
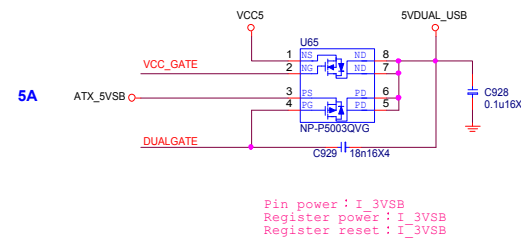
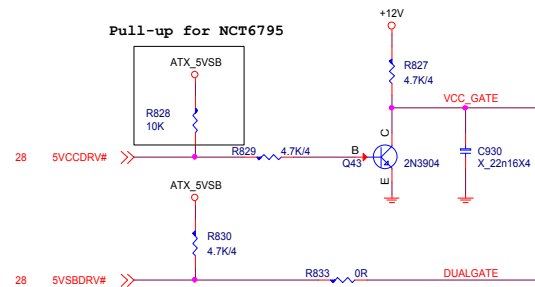
USB2.0  
D0G-0200529-A68 Main  
D0G-0100619-I05 AVL



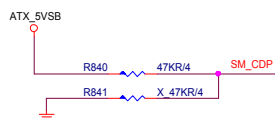
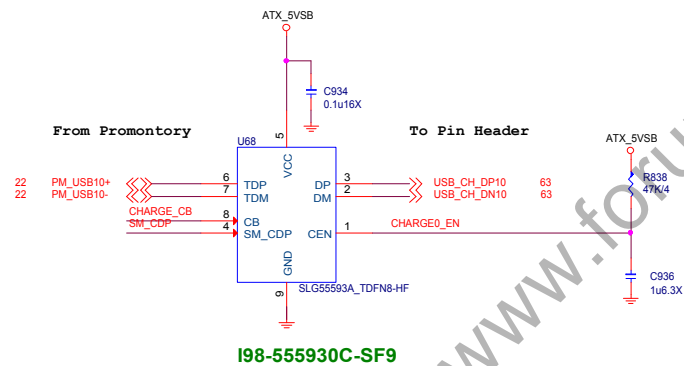
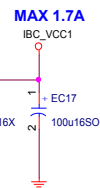
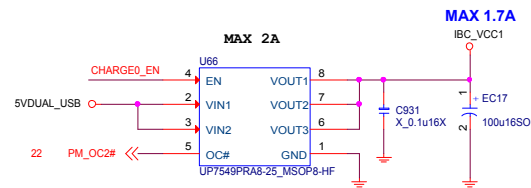
20 PIN CONNECTOR  
BHZXT10[20]#2PITCH\_BLACK-RH-4  
**N32-2101731-AO3**



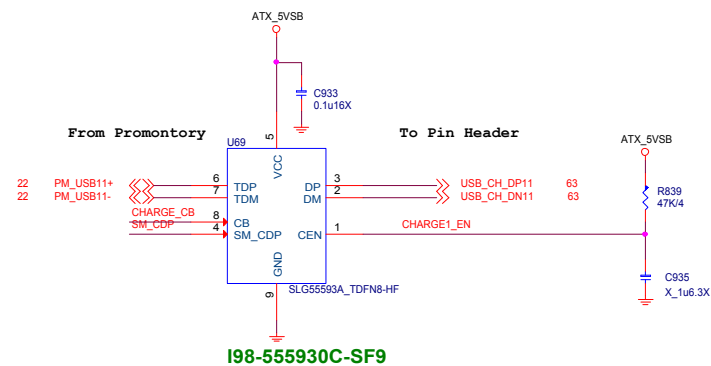
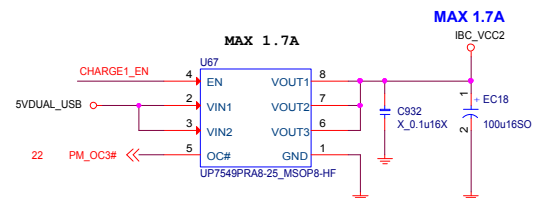
## 5VDUAL\_USB



## USB POWER PORT 0 For USB Charging

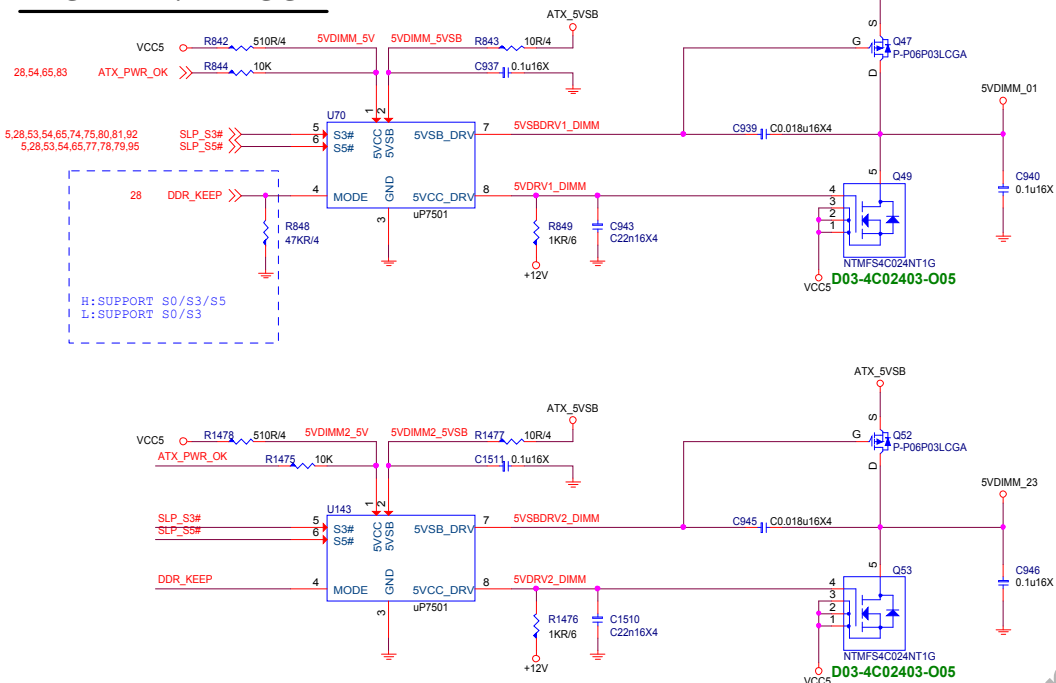


## USB POWER PORT 1 For USB Charging

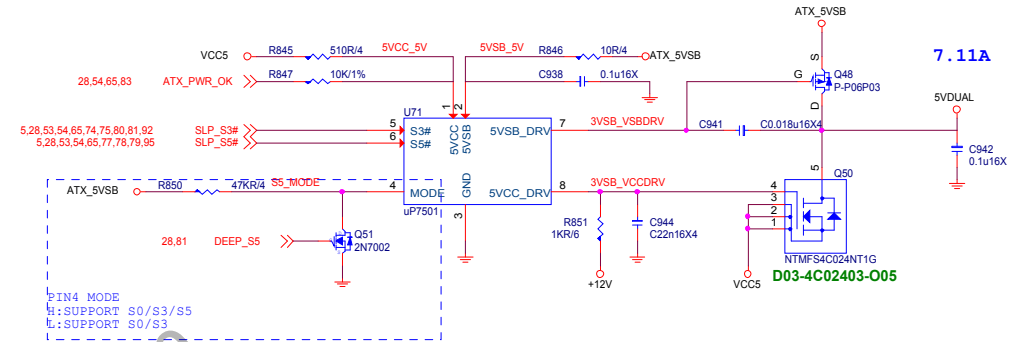




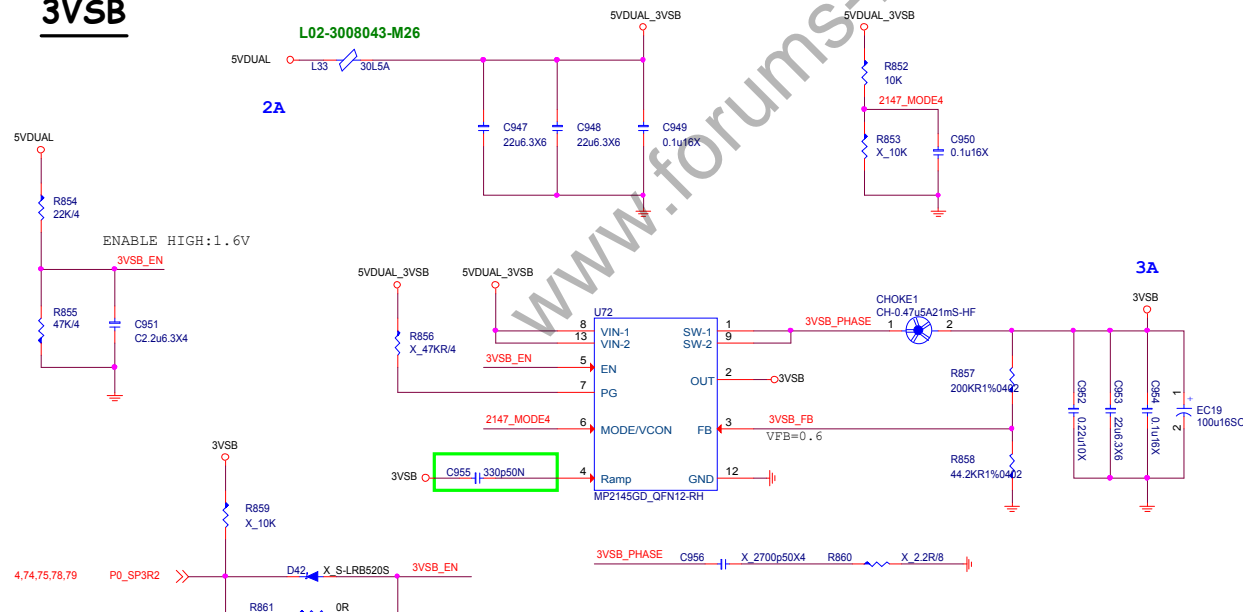
## 5VDIMM FOR DDR



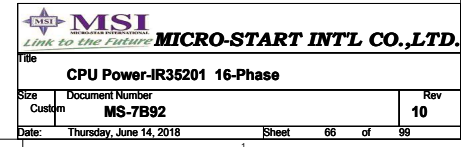
## 5VDUAL For 3VSB、CPU 1.8V



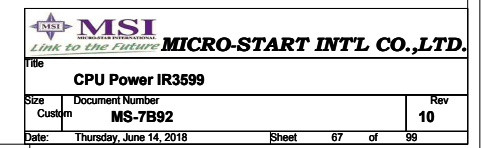
### 3VSB

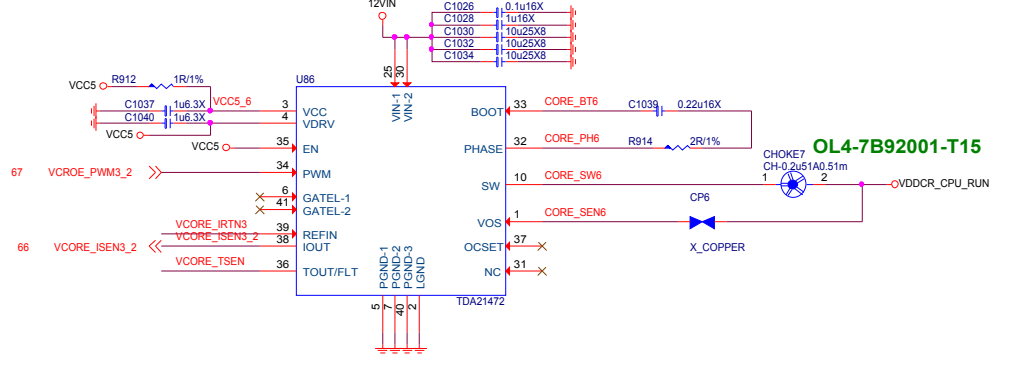
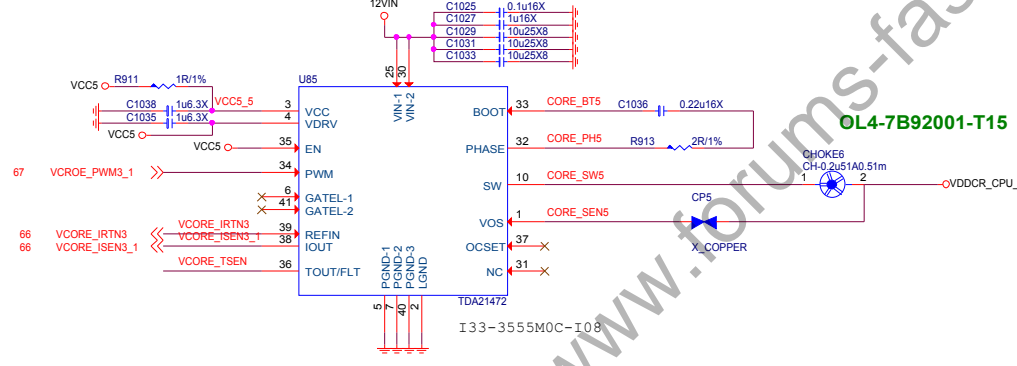
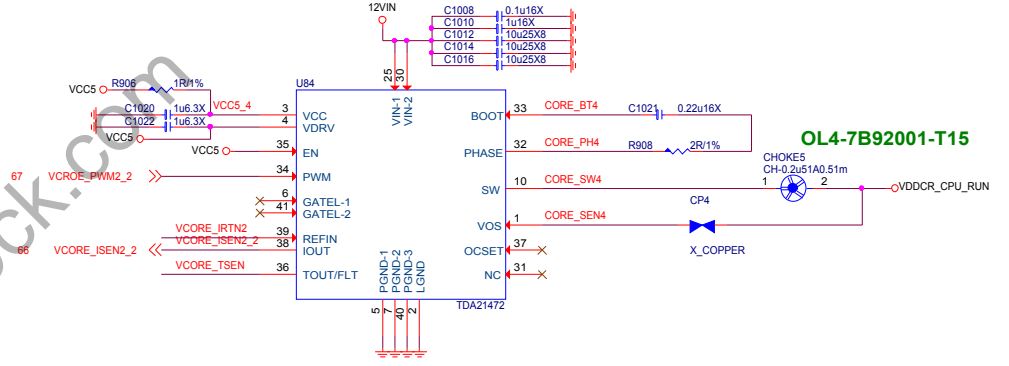
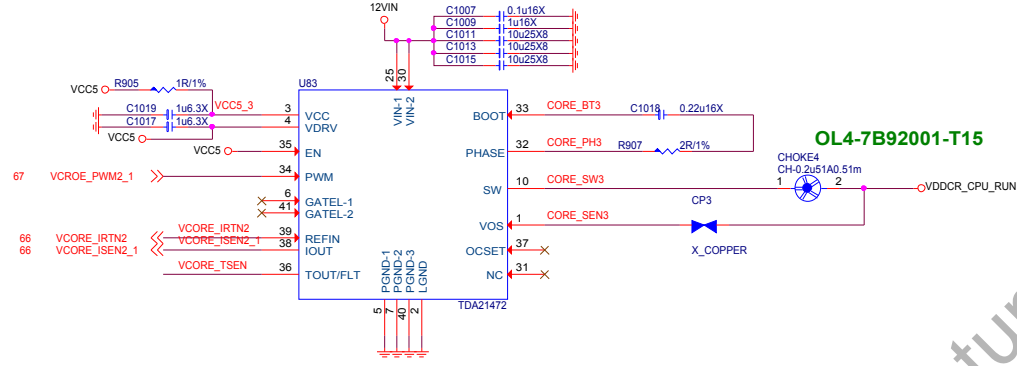
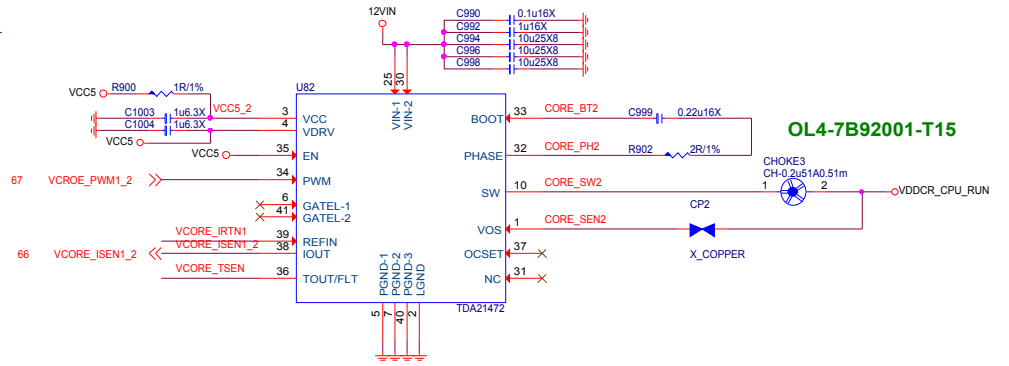
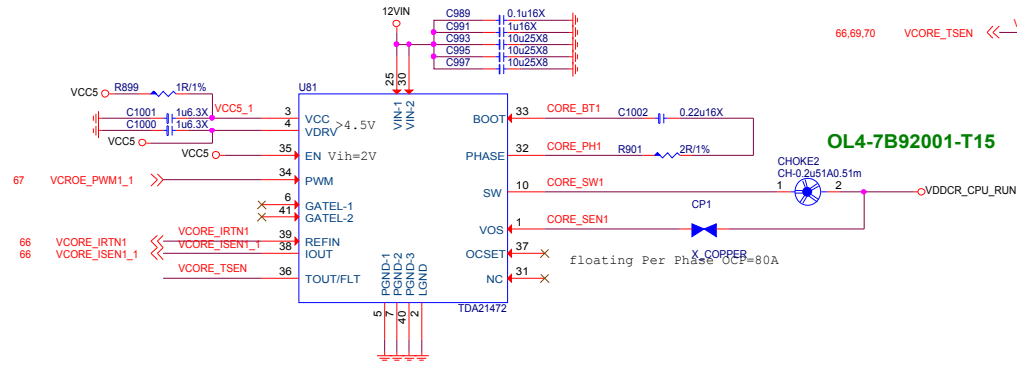


		BOOT VOLTAGE
SVC	SVD	Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

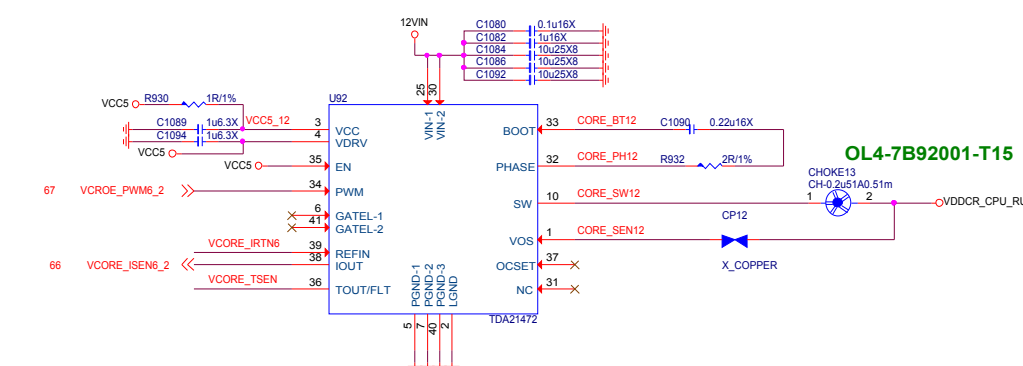
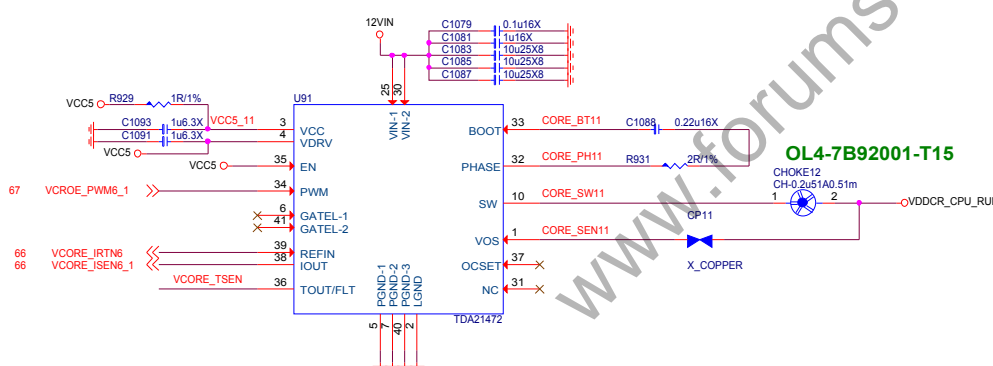
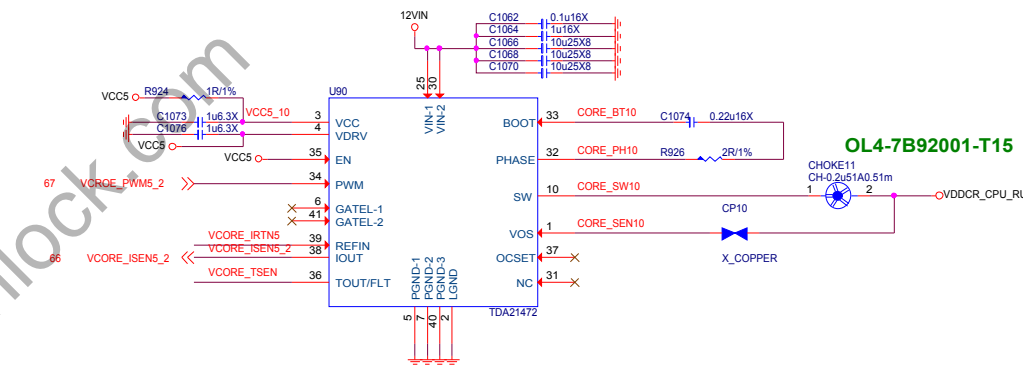
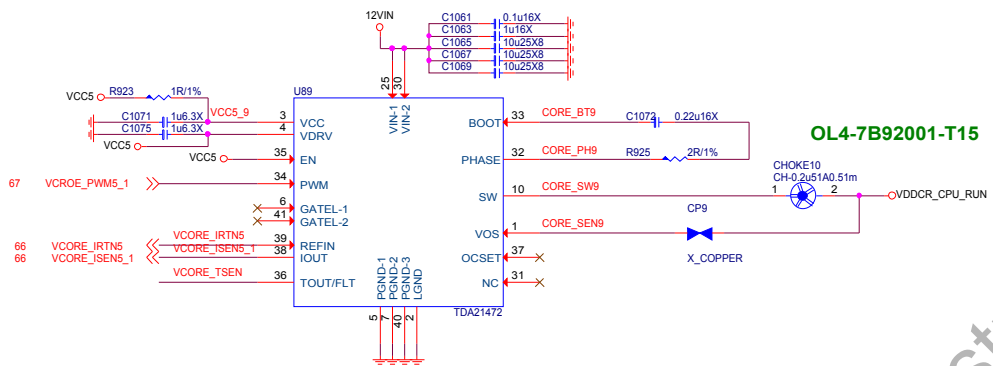
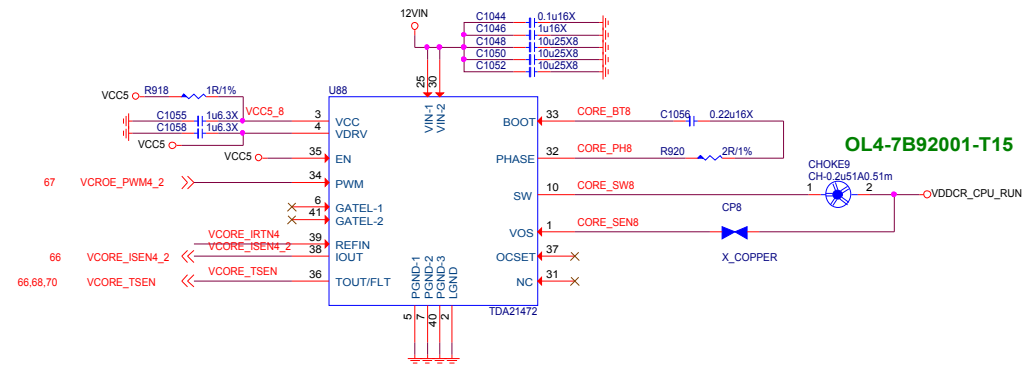
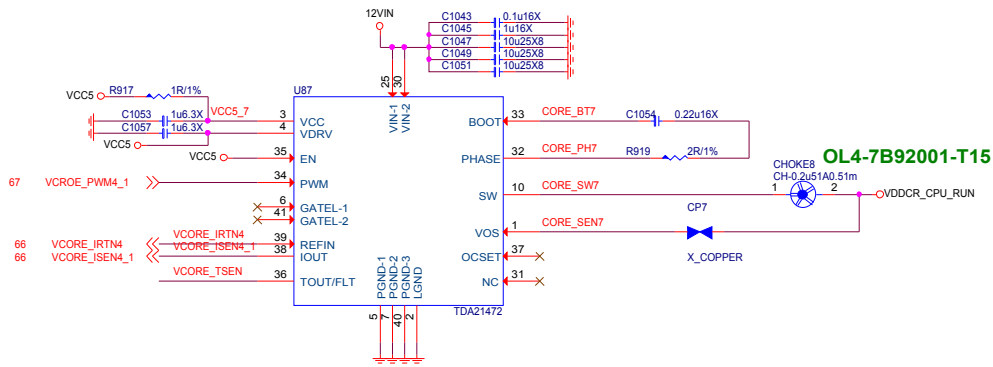


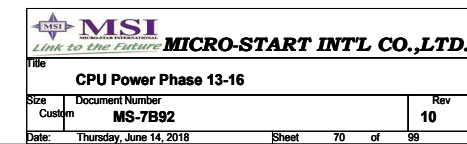
## VCORE Double 16-PHASE





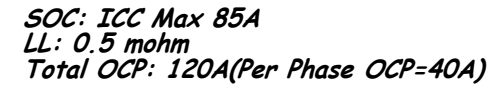
I33-3555M0C-I08





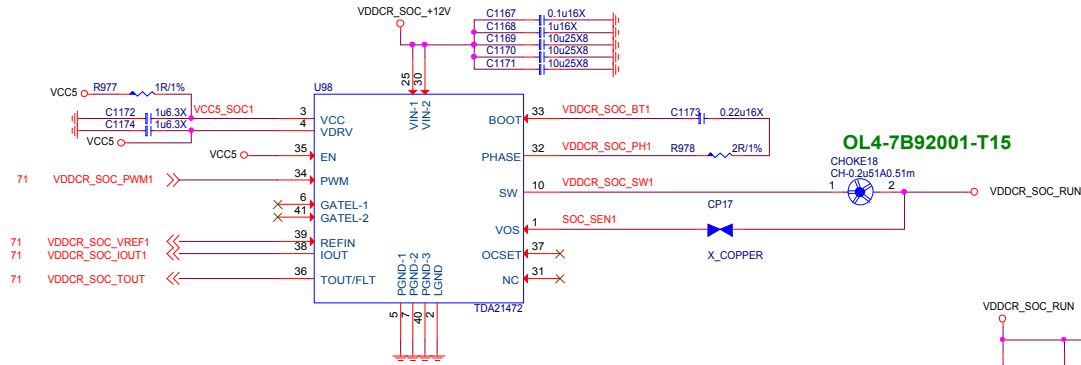
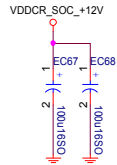
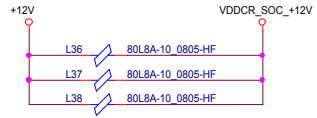
80A  
OCP=120A

		BOOT VOLTAGE
SVC	SVD	Pre PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

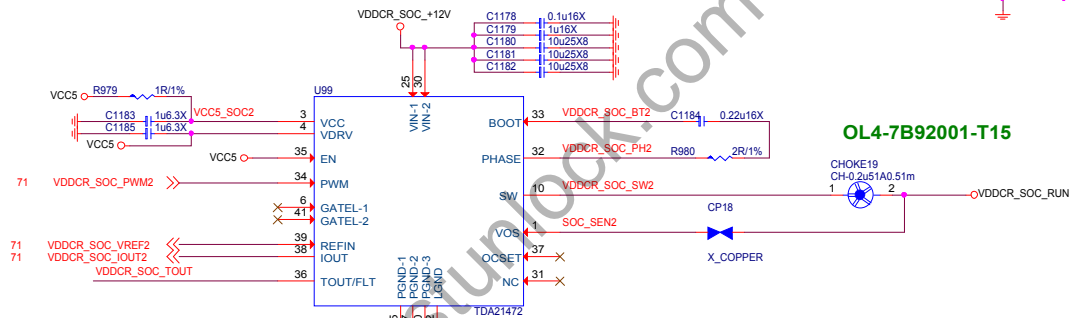
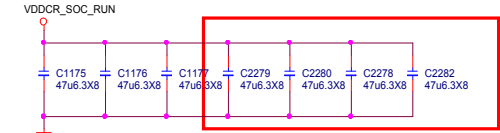


# CPU\_SOC Driver+MOS IC

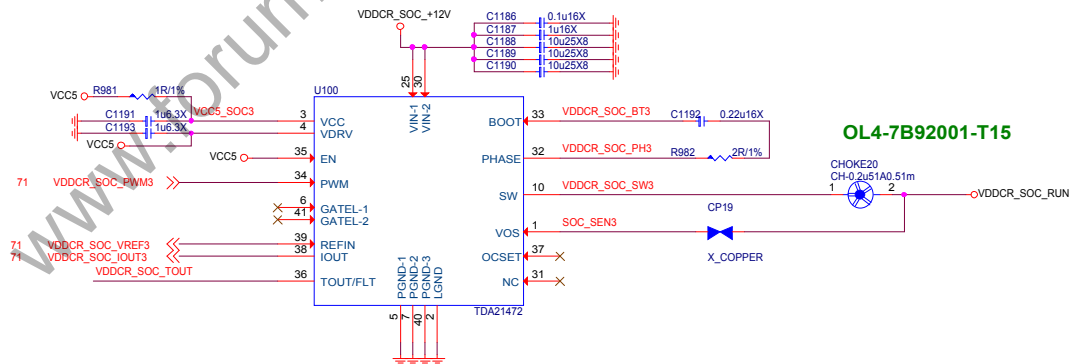
## 3-PHASE



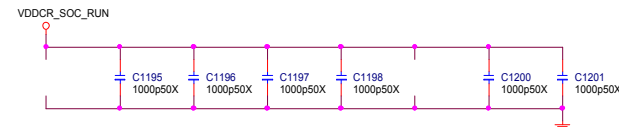
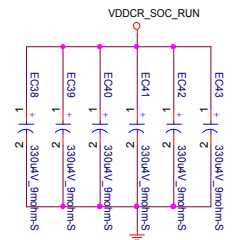
OL4-7B92001-T15



OL4-7B92001-T15



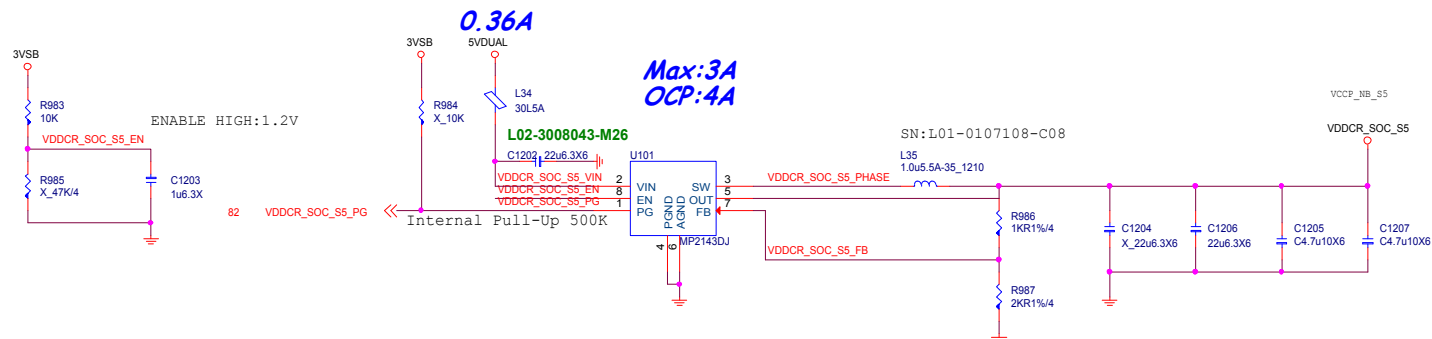
OL4-7B92001-T15





# VDDCR\_SOC\_S5 0.9V

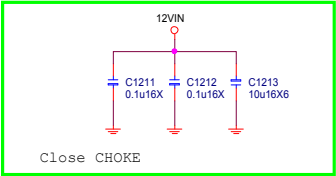
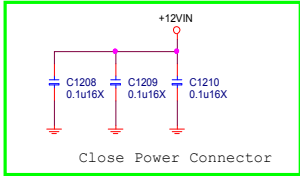
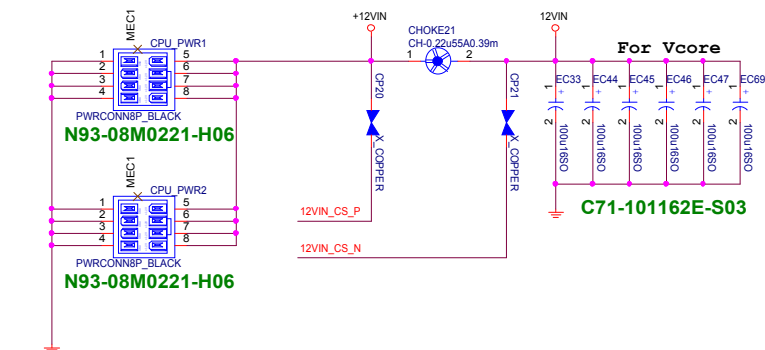
2A



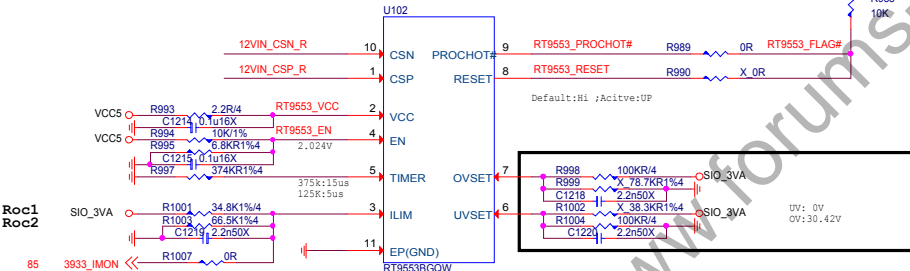
www.forums-fastunlock.com

CPU POWER CONNECTOR

Iripple = 5.6A



RT9553 CURRENT SENSE



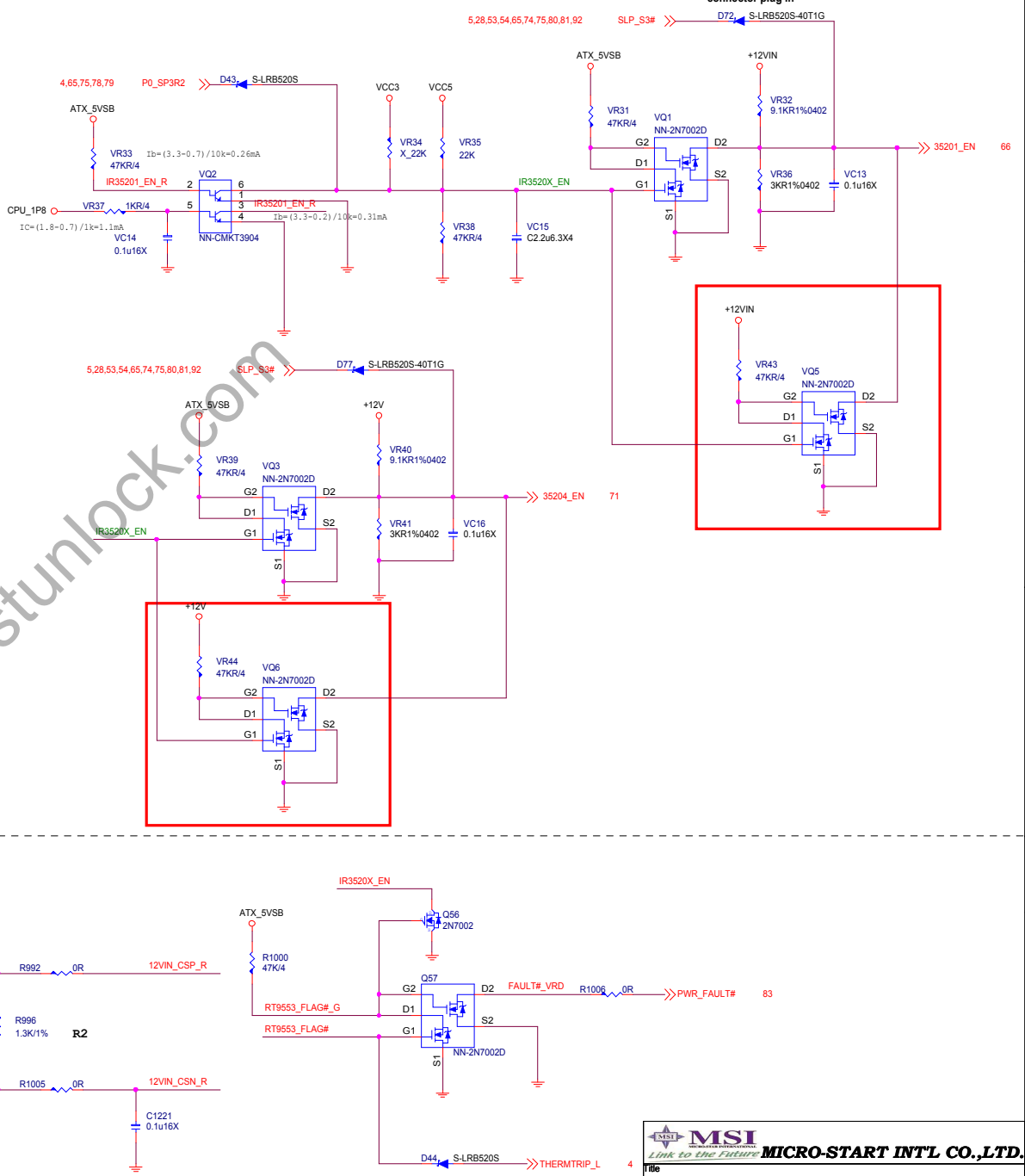
OCP:57A (Without CPU\_SOC PWR)  
Real OCP:57A~73A

$\Delta V_{ILIM} = 10\mu A * [ (34.8K * 66.5K) / (34.8K + 66.5K) ] = 228mV$

$I_{sense} = V_{ILIM} / 100 * R_{sense}$

$\Delta I_{sense} = 228mV / 100 * 0.39m = 5.846A$

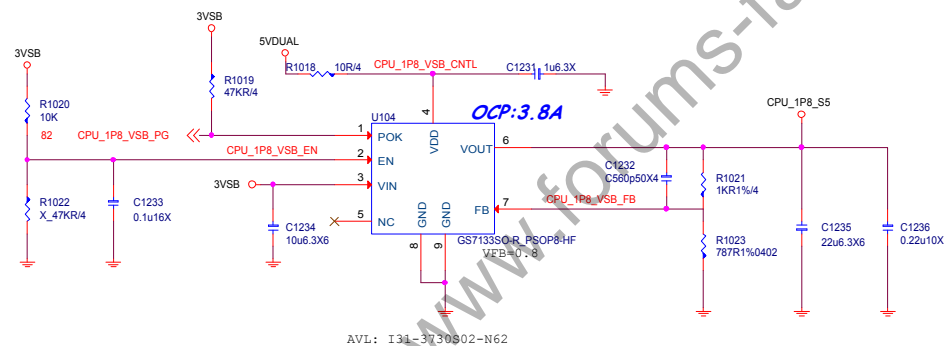
VRM\_Enable circuit



## 3A

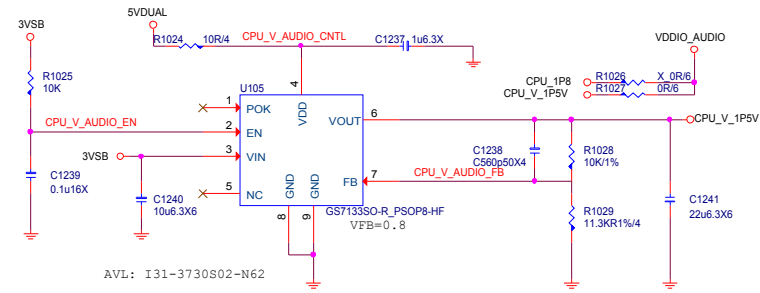


**1A**



# VDDIO\_AUDIO Circuit

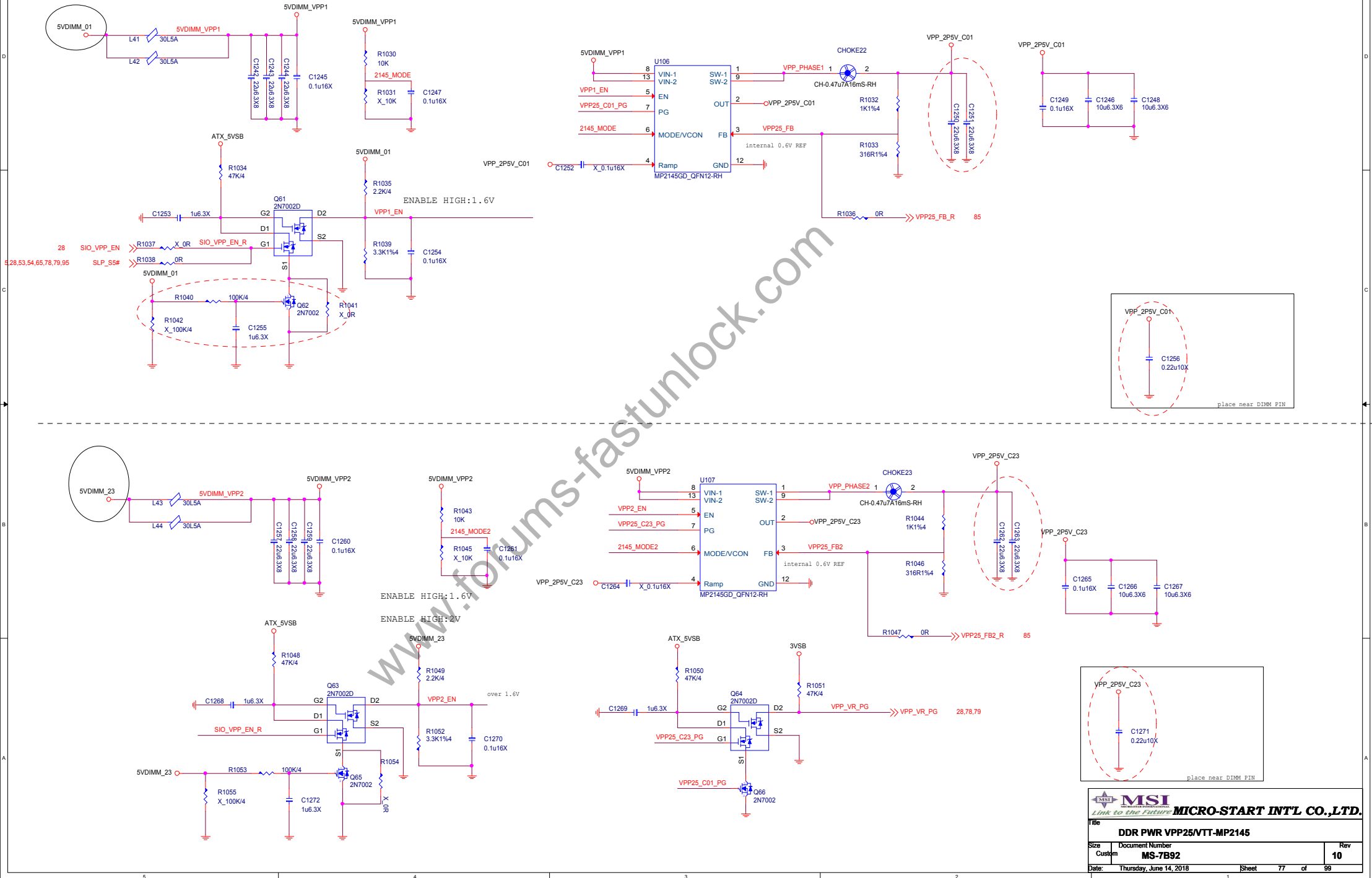
1.5V  
0.25A



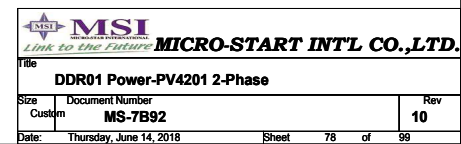
www.forums-fastunlock.com

# 4DIMM :2.24A FOR DDR VPP2.5V

2.5+0.25/-0.125V  
JE3D79 DDR4 max 3V

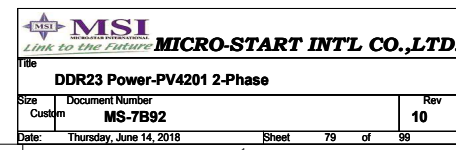


DDR4\_1.2V 15A+9.5A+1.2A=26A  
15A FOR CPU  
9.5A FOR 4DIMM  
1.2A FOR DDR VTT  
OCP: 50A



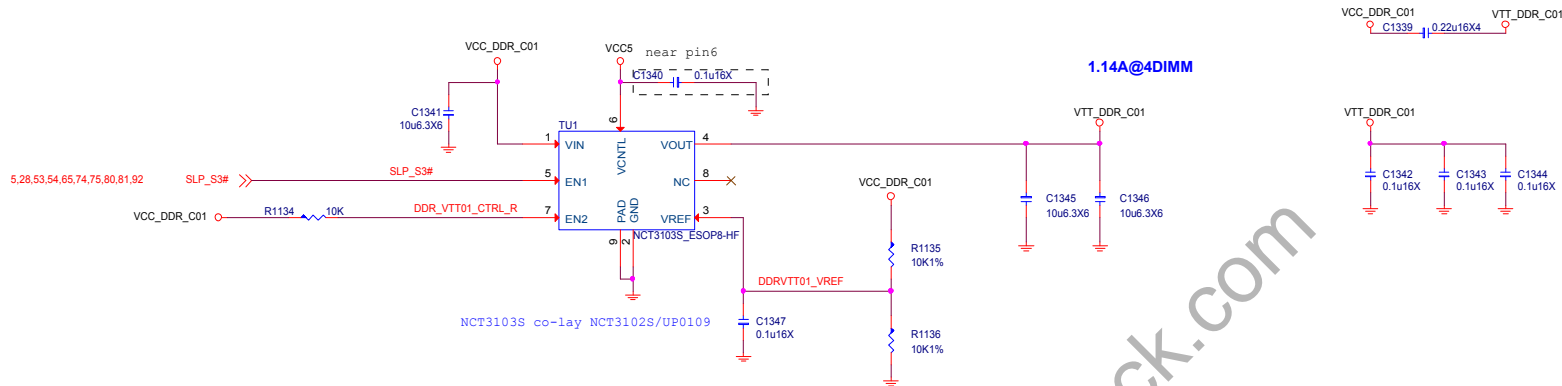
**OCP: 50A**

DDR2\_BOOT1 R1095 2.2R/8 DDR2\_BOOT1\_R C1308 0.1u16X6 DDR2\_PH1A



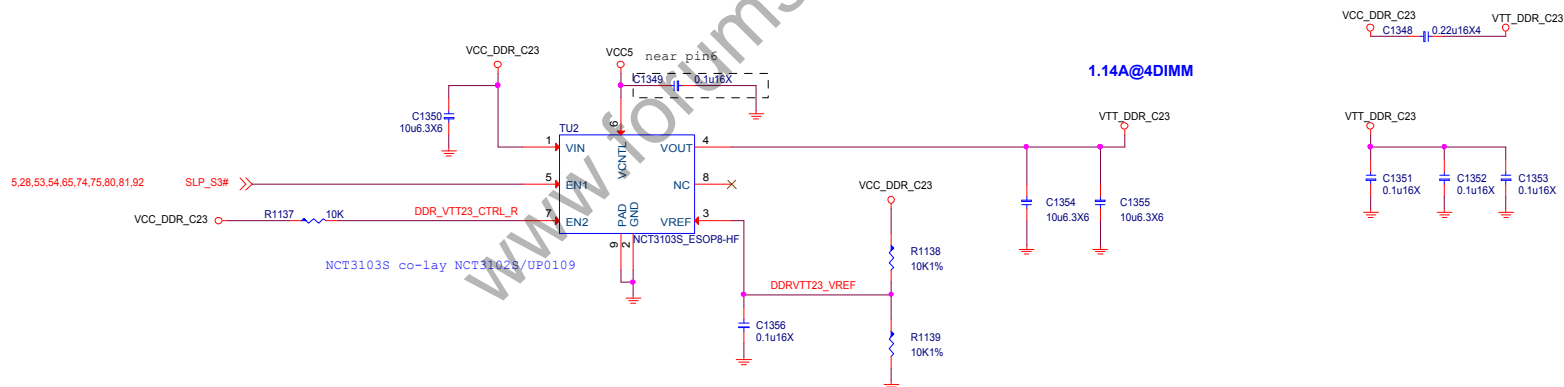
### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



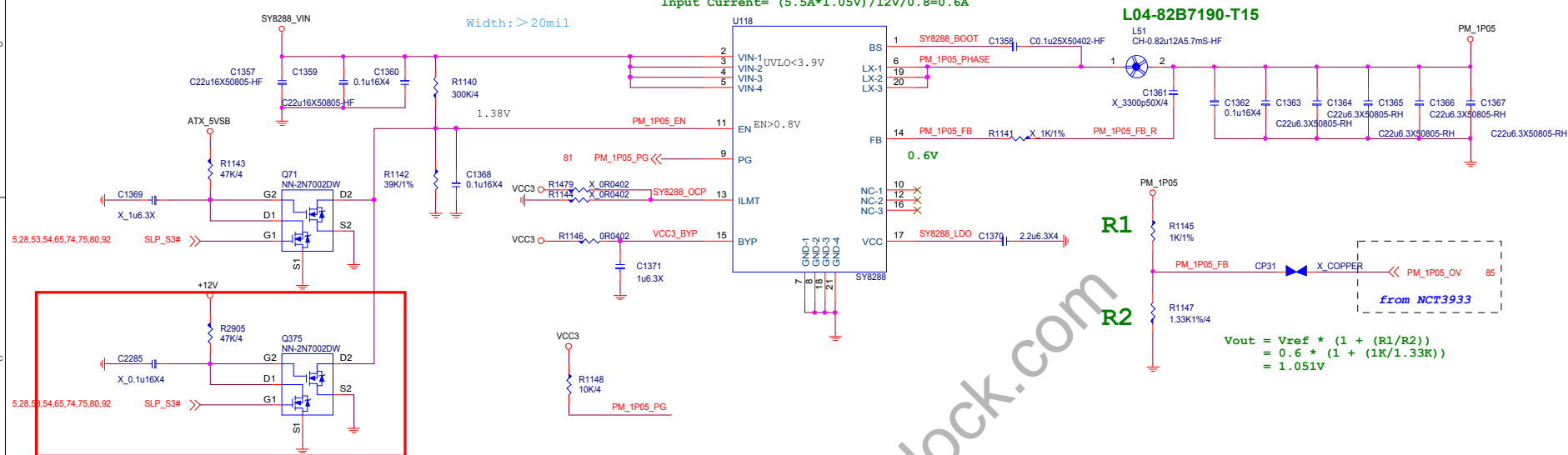
### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



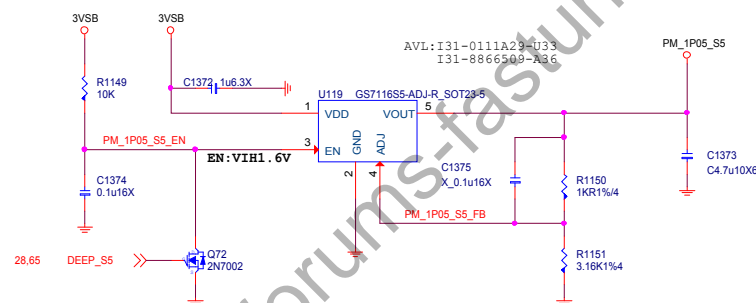


1.05V  
S0:5.5A  
S5:0.05A

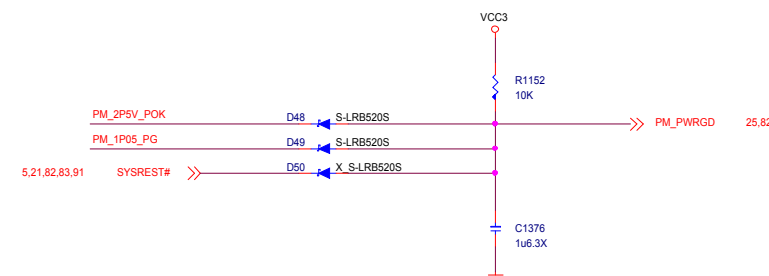
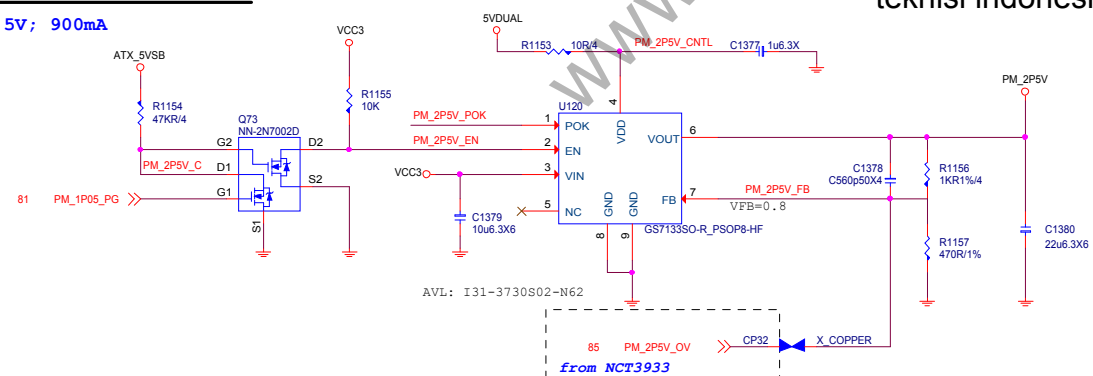


SY8288_OCP	OCP
0	8A
floating	12A
1	16A

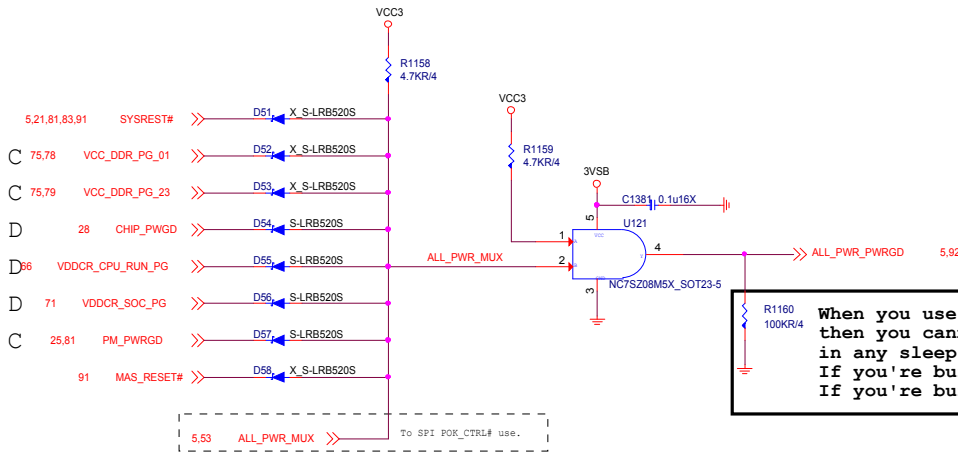
0.05A



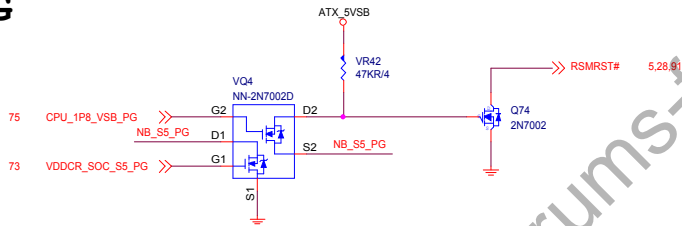
## 2.5V; 900mA



ALL POWER GOOD MUX

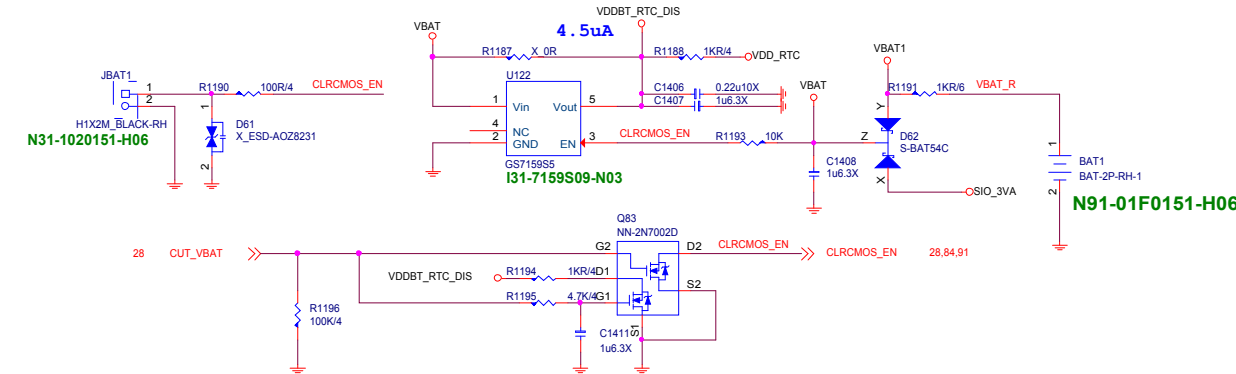


S0 PG  
S5 PG

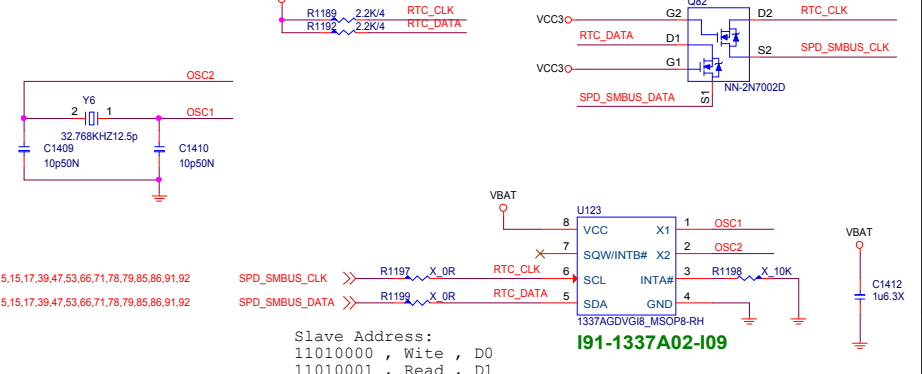




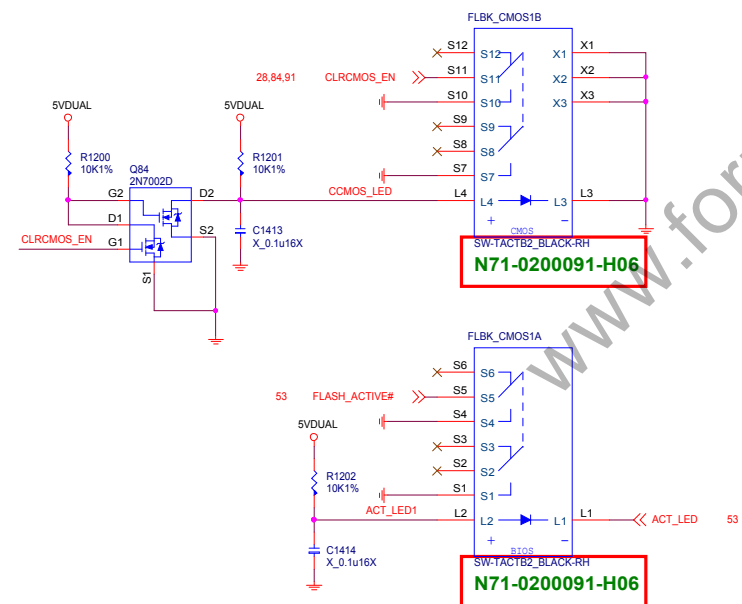
RTC & Clear CMOS Circuit



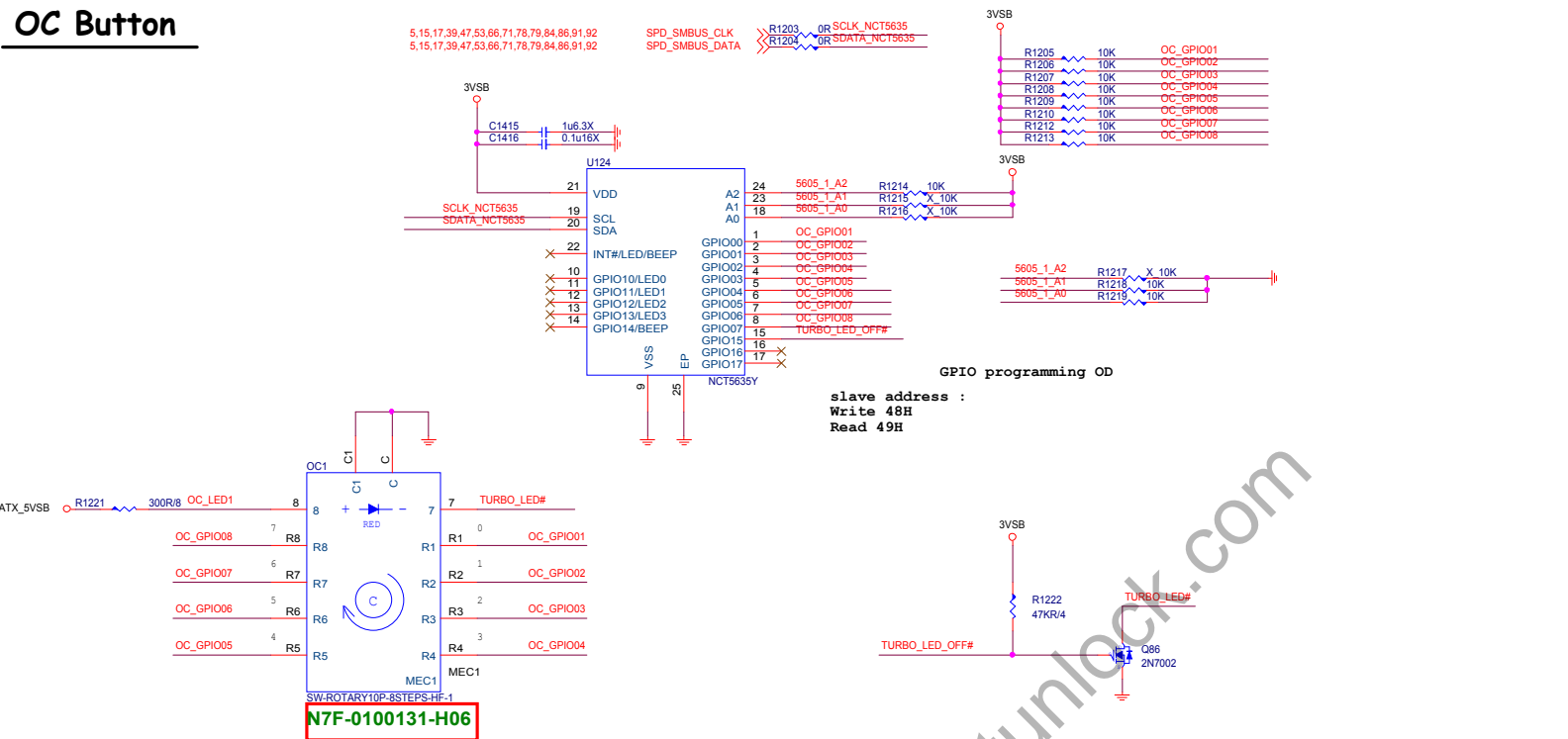
For RTC Backup



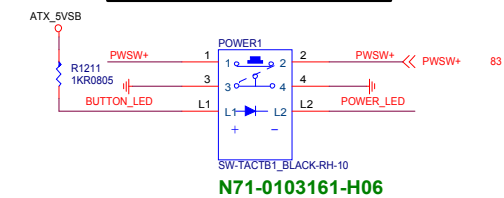
Clear CMOS&Flash Back button



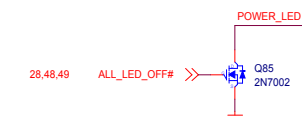
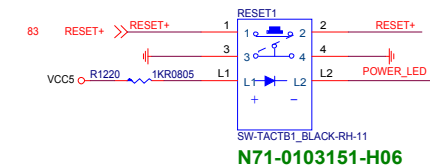
## OC Button



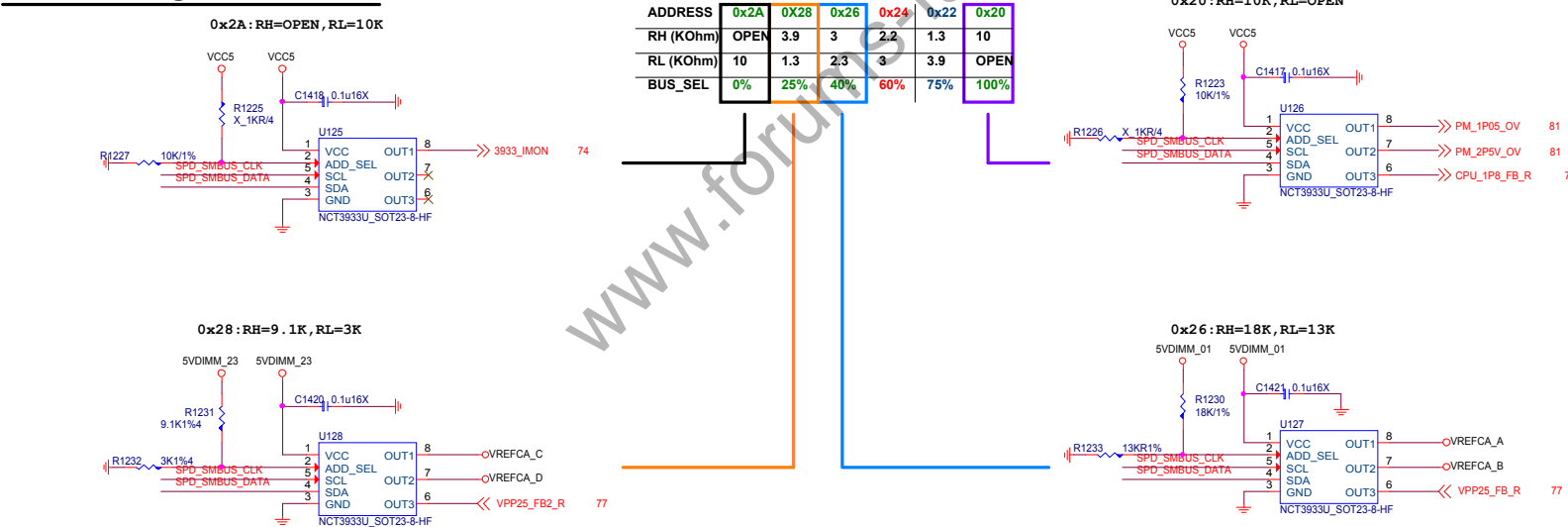
## Power ON Button



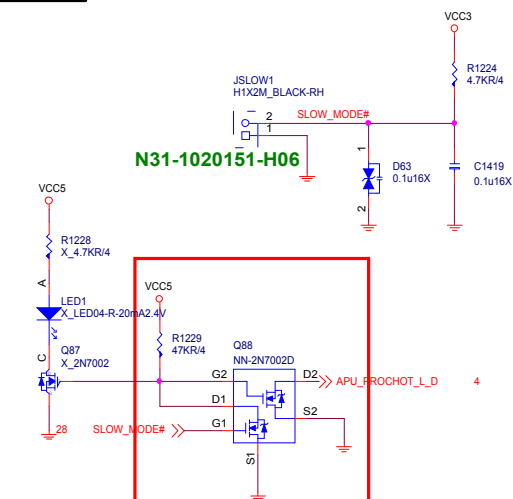
## Reset Button



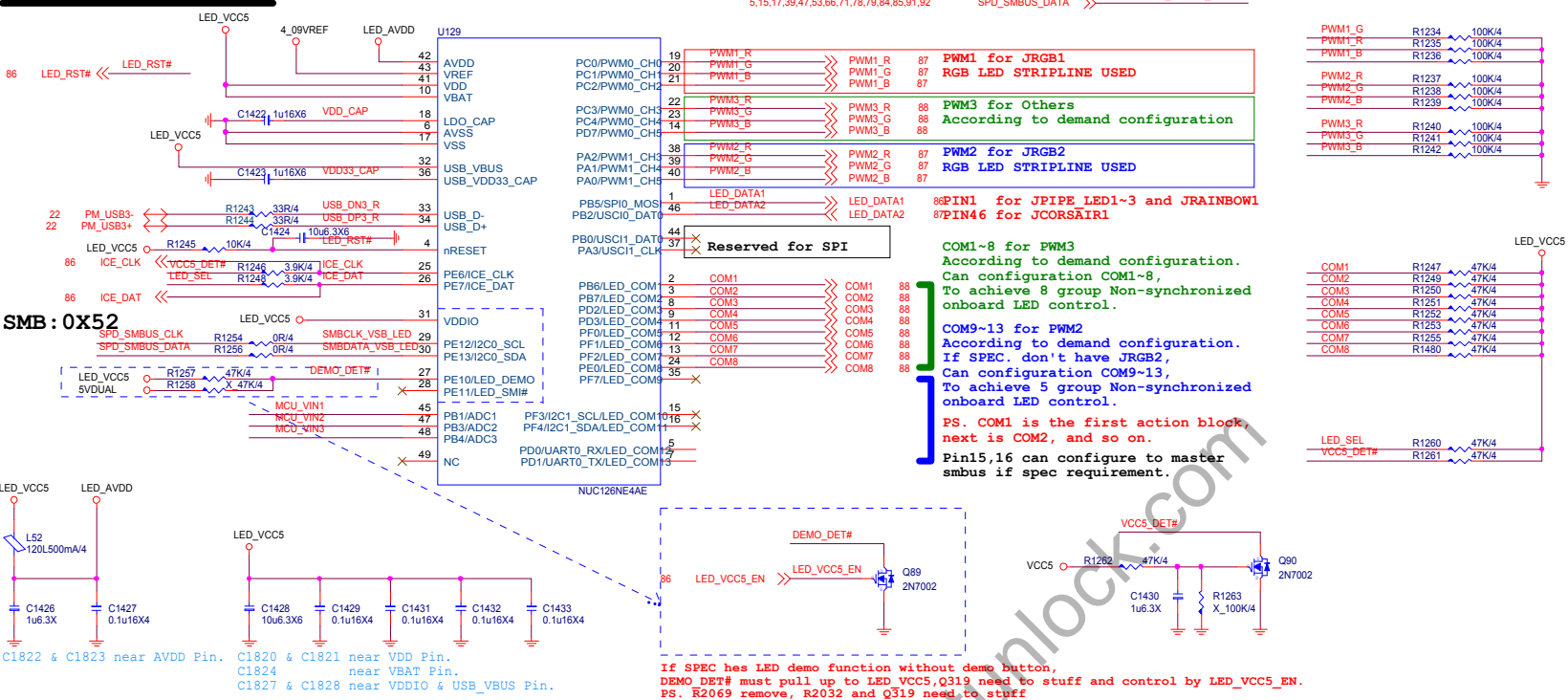
## Over Voltage Control IC



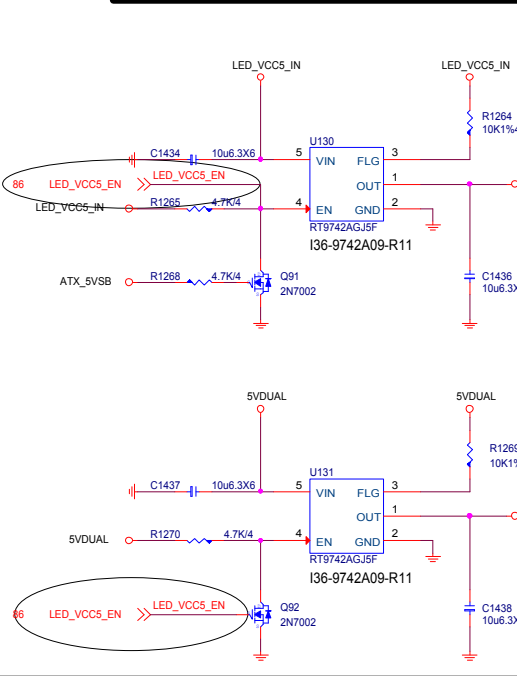
## Slow Mode



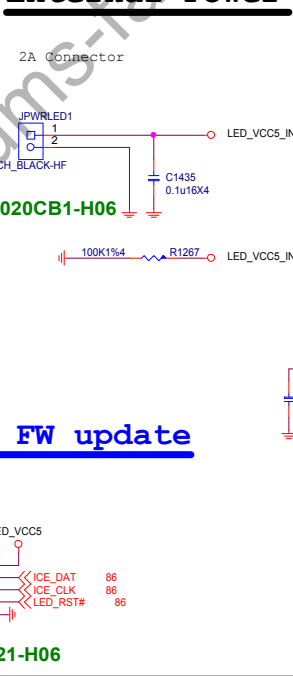
48 PIN LED MCU



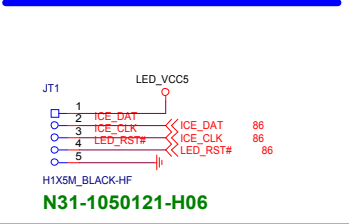
EXTERNAL POWER INPUT



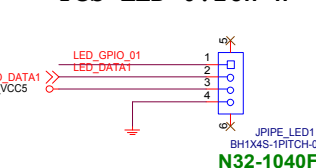
External Power



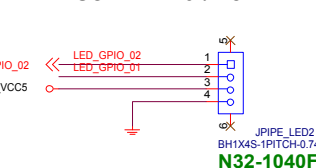
JT1 for FW update



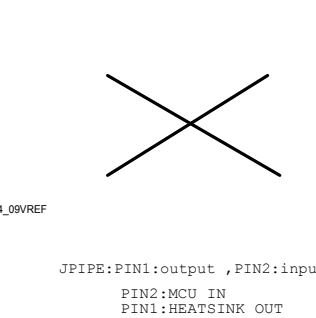
1 PCH HEATSINK LED  
PCS LED\*0.16W=W

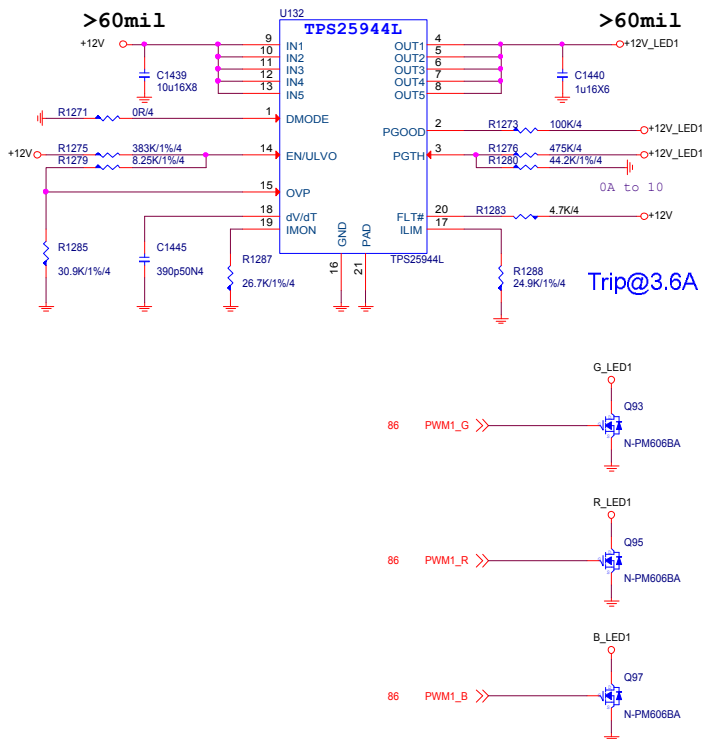


2 AUDIO/IO Cover LED  
PCS LED\*0.16W=W

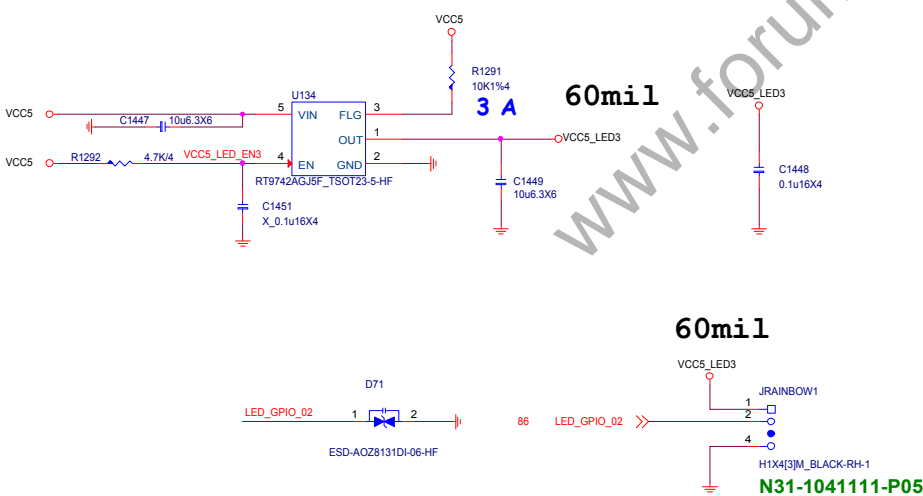
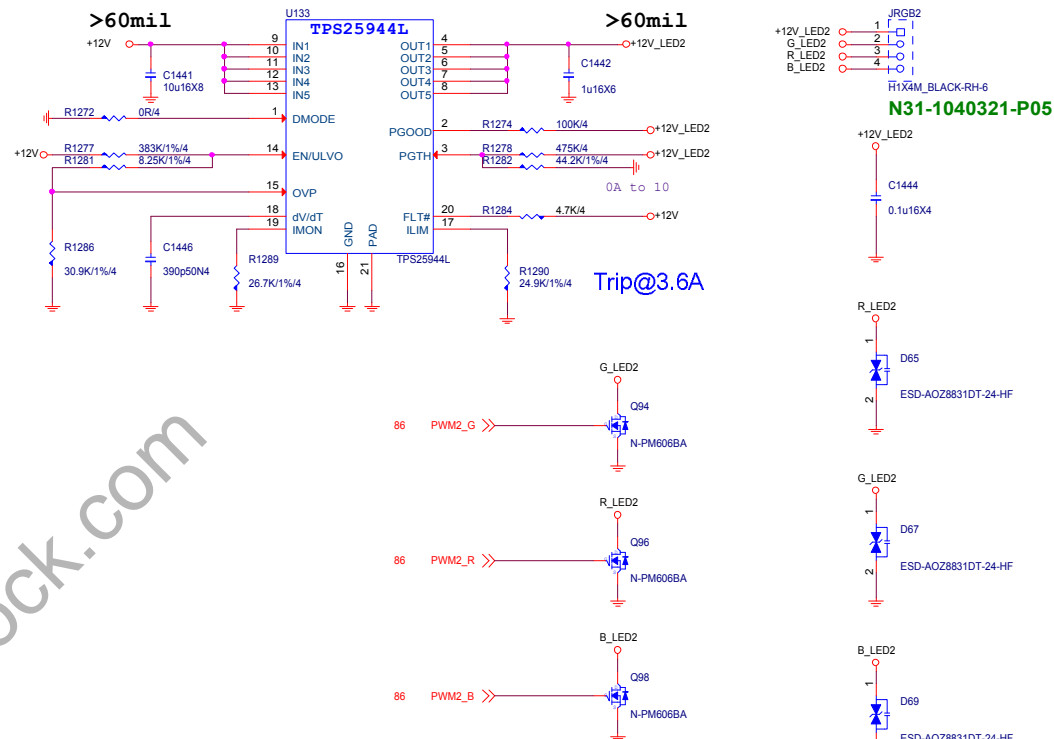


3 MOS HEATSINK LED  
PCS LED\*0.16W=W



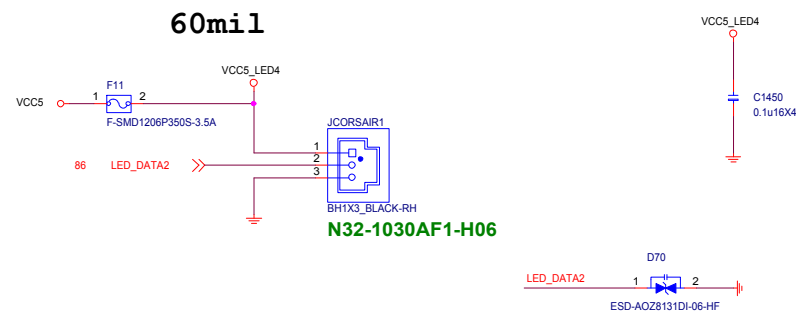
JRGB1

外接LED 燈條 (RGB)   
 --- PCB 文字面 (JRCB1)  
 ---- 手冊註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B), 燈條總輸出電流限制為3安培 (12 伏特)  
 長度限制為2公尺

JRAINBOW1JRGB2

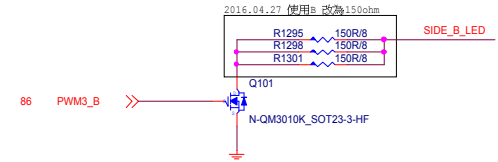
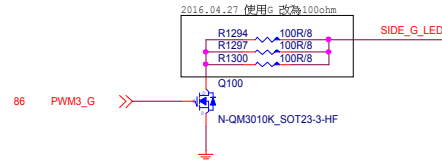
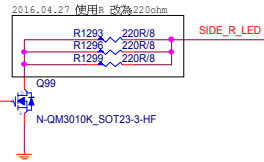
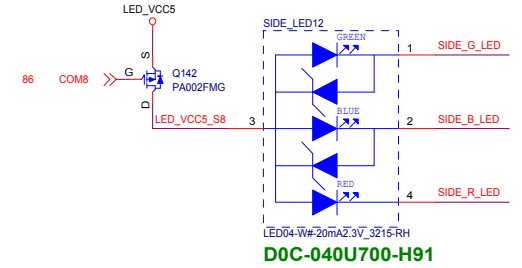
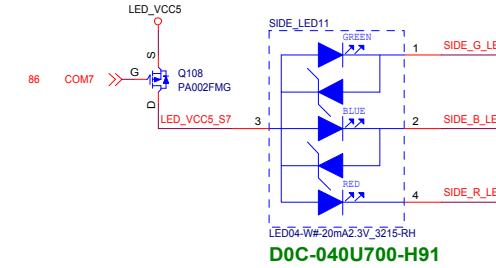
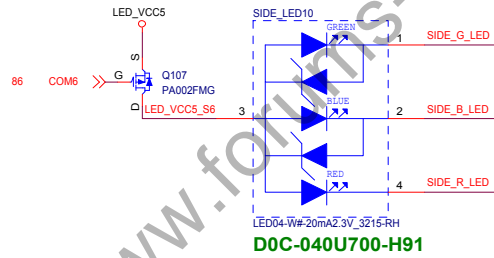
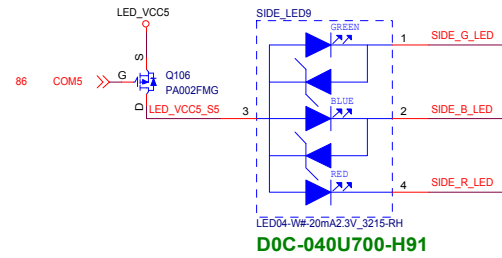
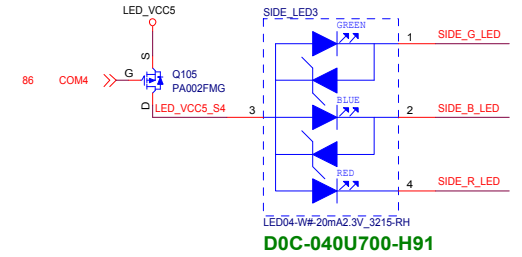
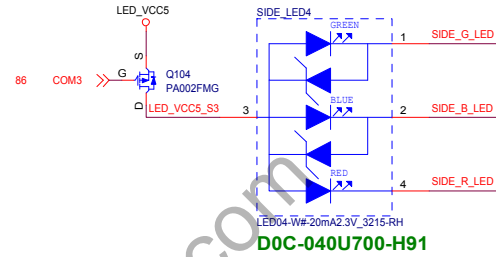
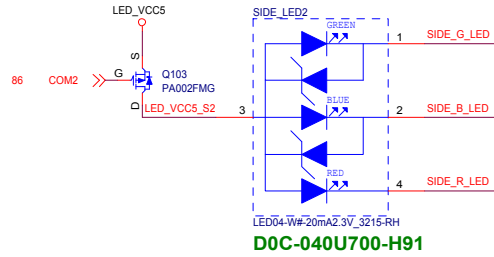
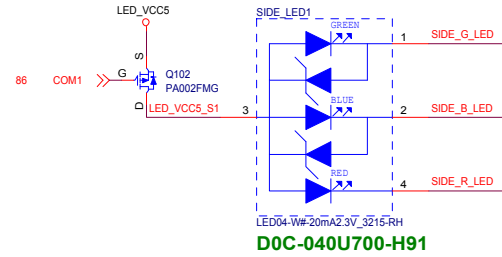
----- 手冊註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JCORSAIR1



<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7B92</b>			
Size Custom	Document Description <b>LED JRGB/JCORSAIR/JRAINBOW</b>	Rev 10	
Date: Thursday, June 14, 2018		Sheet	87 of 99

**BOARD SIDE LED\*8 SET**  
**FORM MCU**



**MICRO-STAR INT'L CO.,LTD**

**MS-7B92**

Size	Document Description	Rev
Custom	<b>LED BOARD SIDE</b>	10
Date:	Thursday, June 14, 2018	Sheet 88 of 99

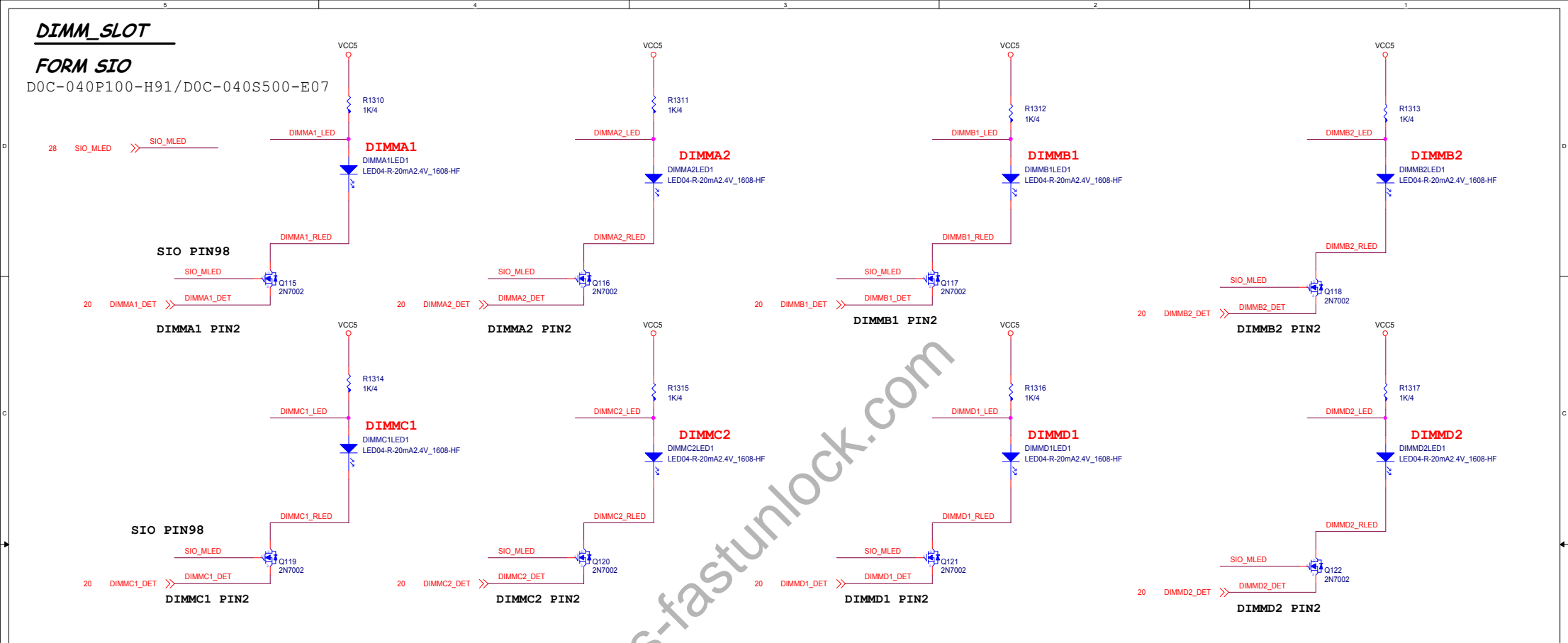


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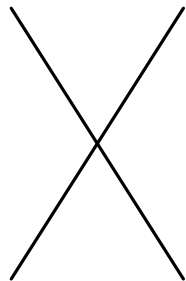
# DIMM\_SLOT

## FORM SIO

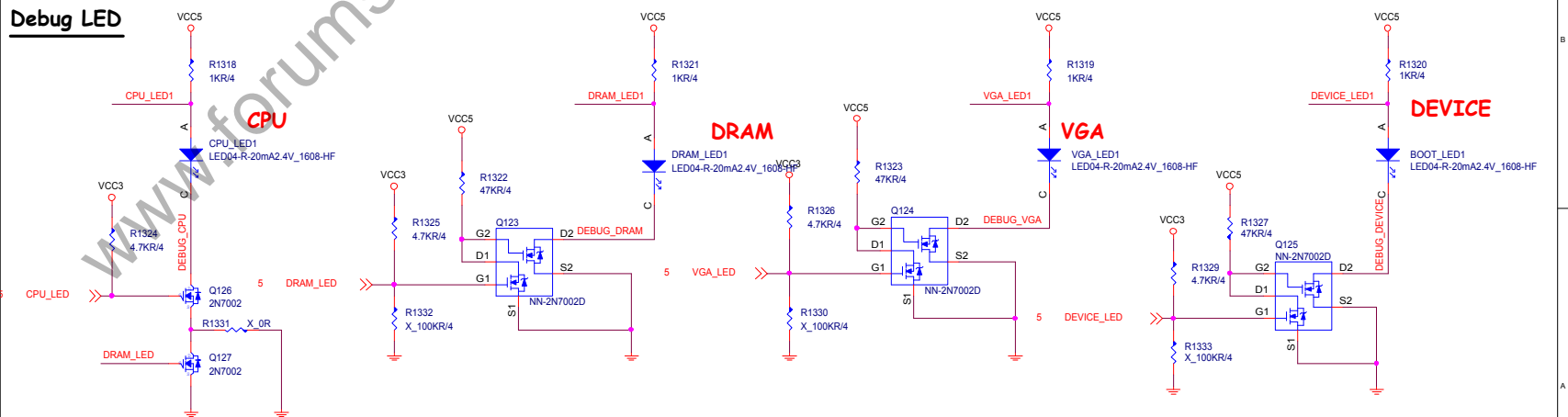
D0C-040P100-H91/D0C-040S500-E07



# AMD AMP Detect LED




## Debug LED



LED	GPIO	AGPIO84 0	AGPIO85 0	EGPIO84 1	EGPIO85 1
亮		GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅		GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

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MICRO-START INTL CO.,LTD.

File

Size

Custom

Document Number

MS-7B92

Rev

10

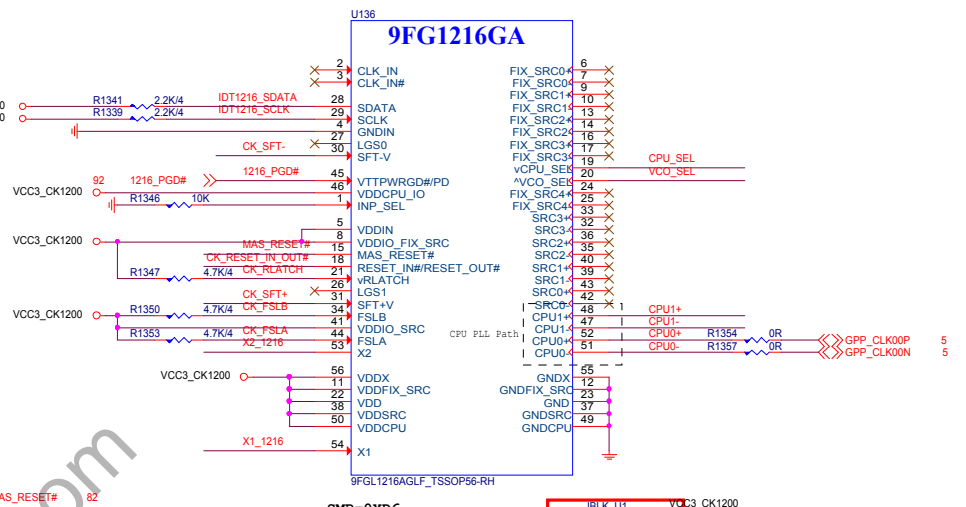
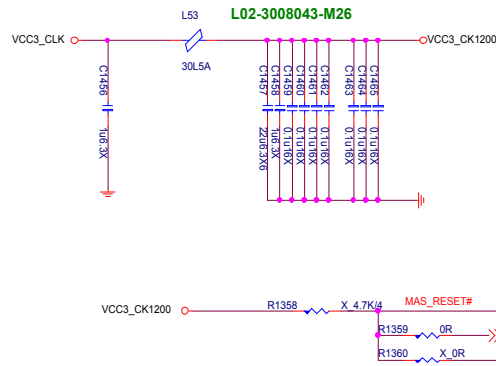
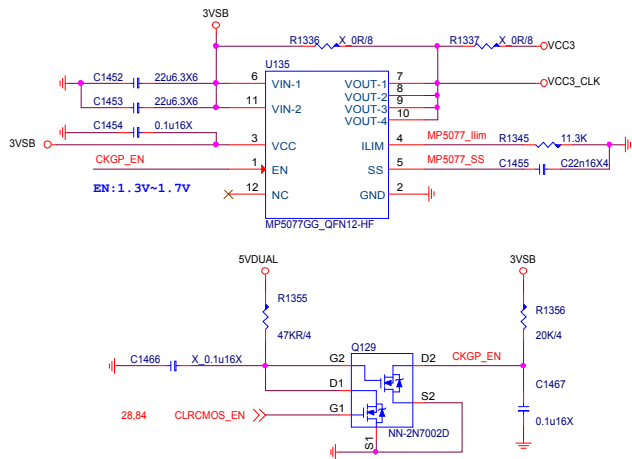
Date

Thursday, June 14, 2018

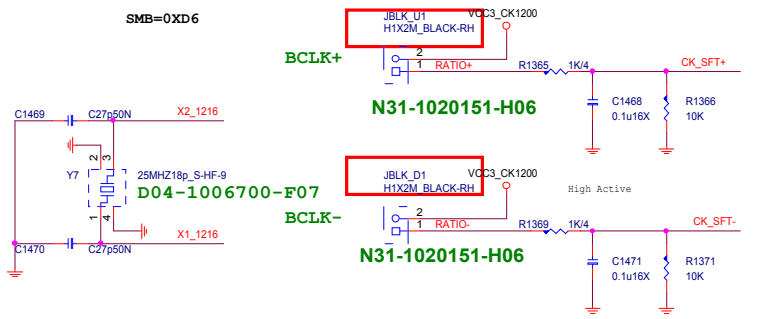
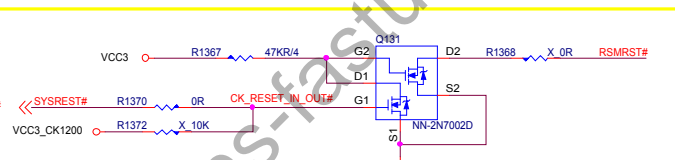
Sheet

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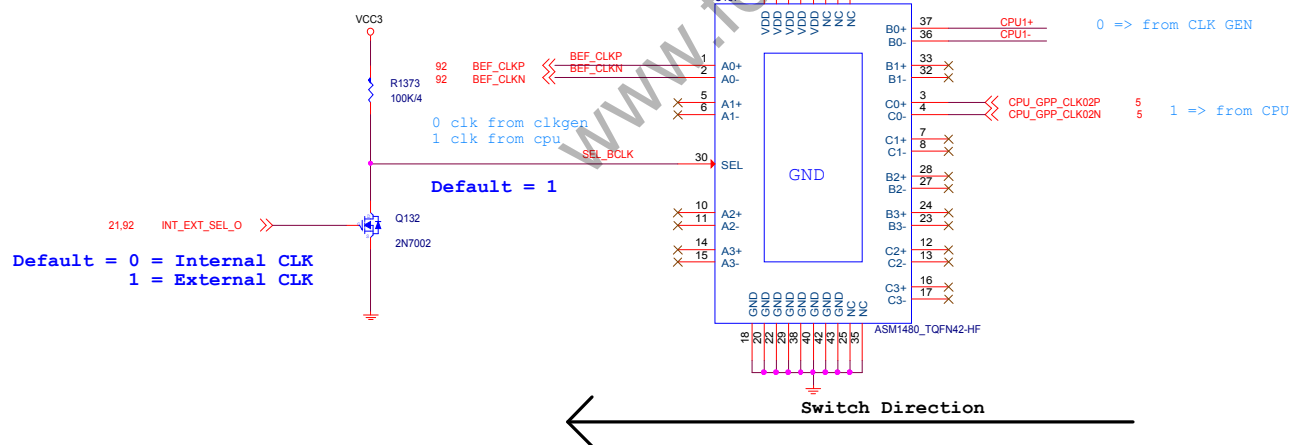
# CLOCK GEN



Input latch pin to select CPUCLK PLL source.  
0 = SRC PLL (default), 1 = CPU PLL



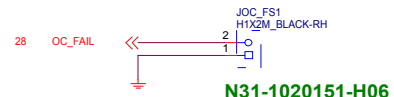
# CLOCK SWITCH



# OC Retry Button



# OC Fail Setting Button



## CLOCK BUFFER

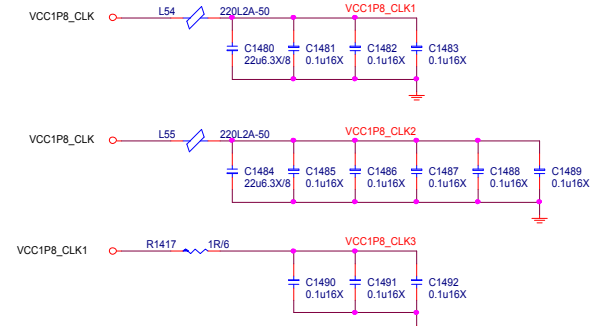
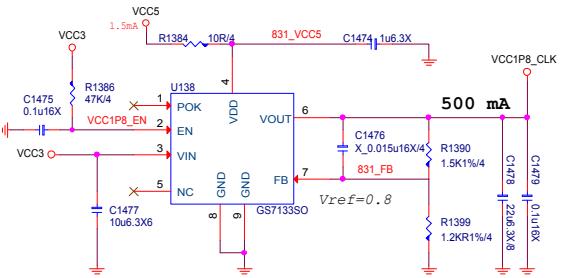
5,15,17,39,47,53,66,71,78,79,84,85,86,91  
5,15,17,39,47,53,66,71,78,79,84,85,86,91

SPD\_SMBUS\_CLK  
SPD\_SMBUS\_DATA

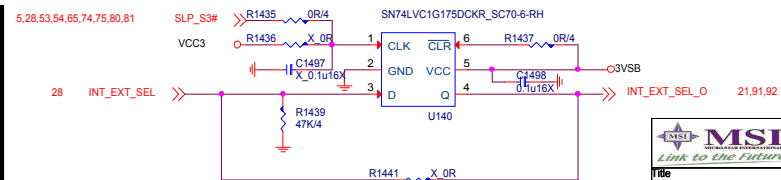
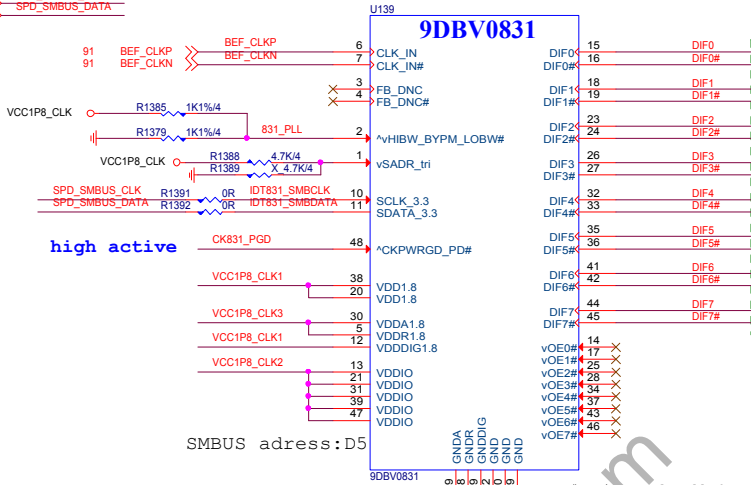
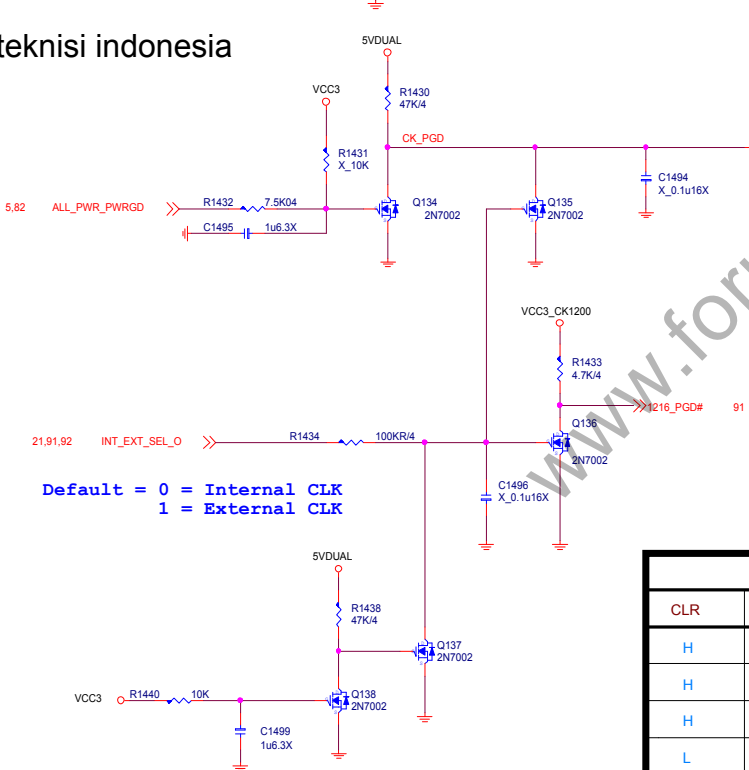
```



SPD_SMBUS_CLR
SPD_SMBUS_DATA

```

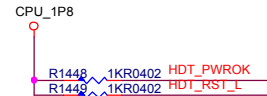
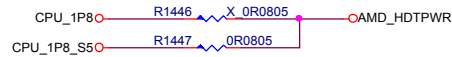


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INPUTS			OUTPUTS
CLR	CLK	D	Q
H		L	L
H		H	H
H	H or L	X	Qo
L	X	X	L

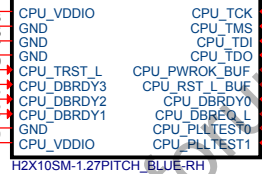
Stuff for first model



AMD\_HDTPWR

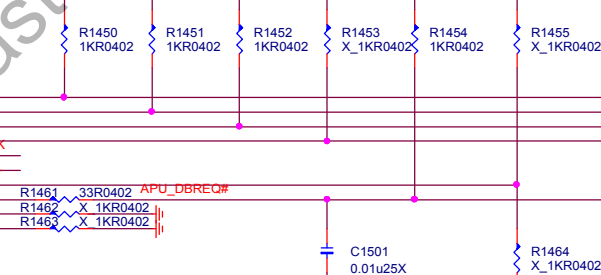
AMD\_HDTPWR

AMD\_HDT1



CPU\_1P8

AMD\_HDTPWR



$$IB = (AMD\_HDTPWR - V_{be}) / 4.7k$$
$$(1.8 - 0.95) / 4.7k = 0.181mA$$

$$IC = (V_c - V_{ce}) / 10k$$
$$(1.8 - 0.2) / 10k = 0.16mA$$

$$IB = (V_b - V_{be}) / 10k$$
$$(1.75 - 0.95) / 10k = 0.08mA$$

$$IC = (V_c - V_{ce}) / 10k$$
$$(3.3 - 0.2) / 10k = 0.16mA$$

$$B * Ib > Ic = 10 * 0.181 = 1.81 > 0.16$$

$$B * Ib > Ic = 10 * 0.08 = 0.8 > 0.16$$

$$IB = (AMD\_HDTPWR - V_{be}) / 4.7k$$
$$(1.8 - 0.95) / 4.7k = 0.181mA$$


$$IC = (V_c - V_{ce}) / 10k$$
$$(1.8 - 0.2) / 10k = 0.16mA$$

$$IB = (V_b - V_{be}) / 10k$$
$$(1.75 - 0.95) / 10k = 0.08mA$$

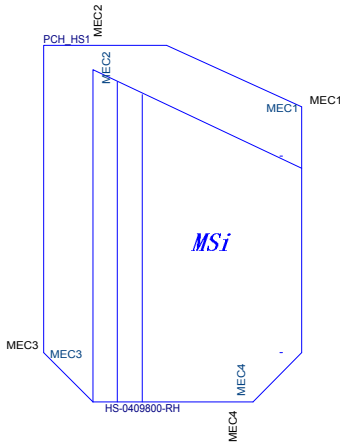
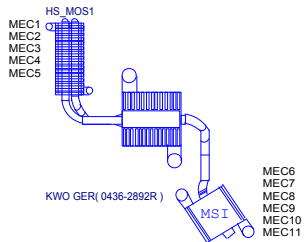
$$IC = (V_c - V_{ce}) / 10k$$
$$(3.3 - 0.2) / 10k = 0.16mA$$

$$B * Ib > Ic = 10 * 0.181 = 1.81 > 0.16$$

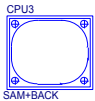
$$B * Ib > Ic = 10 * 0.08 = 0.8 > 0.16$$

 <b>MICRO-START INT'L CO.,LTD.</b>		
Title		
<b>APU HDT DEBUG</b>		
Size	Document Number	Rev
	<b>MS-7B92</b>	<b>10</b>
Date:	Thursday, June 14, 2018	Sheet 93 of 99

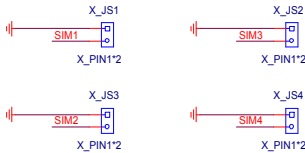
HEAT SINK



CPU Socket



Simulation



MANUAL PART

AMI1

AMI LABEL

G51-M1SPXXA-A09

CFOS1

Label

CFOS

Y02-MU00170-CFO

NAHIMIC1

Label

NAHIMIC

Y02-MU00100-NAH

SLI1

Label

SLI

Y01-RNVIDIN-000

MKT1

Label

X\_MKT

G51-M1SPL82-Q13

XSPLIT1

Label

X\_XSPLIT

Y02-MA00401-XSP

SSE1

Label

X\_SSE

Y02-MA00101-SSE

BAT1\_X1

BAT-CR2032-RH

D06-0100101-P01

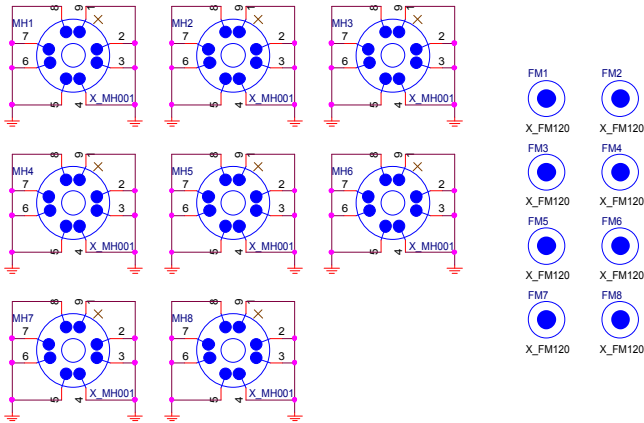
PCB1

7B92-1.1

PD0-07B9211-G37, 精成-深圳, 204, 寶安恩斯邁廠 (MSIS)

PD0-07B9211-G37, 精成-深圳, 1, 台北微星廠 (MSI)

Optics Orientation Holes



Add for EMI

